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Performance vs. Power Analysis for Optimal Point of a Semiconductor Technology

Yuhan Guo

WLSA Shanghai Academy, Shanghai, China

Abstract: *The sustainability of power for the portable electronic devices is the key issue in the modern technical products. Besides the battery capacity, the other root cause in sustainability is the power consumption of the integrated circuits (IC) chip inside the devices. The reduction of the power consumption is an important topic in the IC design industry. This paper is based on our project in the Microelectronic Club. Combining the analysis technique learned in the club and our basic knowledge in transistor from the physics class, the power of transistor circuits are calculated. Besides, lowering the power will also slow down the speed of ON-OFF switch in the transistors, therefore, to find an optimal point for the operating voltage with balanced performance vs. power is our goal. We present the result of our computer simulation and the analysis process, also suggest the optimal voltage some the applications with this semiconductor technology.*

Keywords: *Semiconductor Technology, Logic Gates, Performance, Propagation Delay, Power Consumption, Simulation Results*

1. Introduction

The motive of this research is from our curiosity about the battery life in the portable devices such mobile phone, Bluetooth earphone, smart watch, etc. It is intuitive that reducing the power is as important as increasing the power storage in the battery, and our study is focused on the power reduction of mobile devices for longer battery life.

We have learned some basic knowledge on semiconductor from the textbooks [1][2] of physics such as n-type and p-type material, diode, forward and reverse bias, transistor, integrated circuits (IC) chip on semiconductor wafer, etc. These semiconductor background was also previewed and reinforced in our Microelectronics Club which is a good extracurricular activity and knowledge supplement. First, the concept of binary system was introduced in the club, then we learned the basic elements of digital circuits[3]. Since the basic elements, i.e., the digital gates such as AND, OR NOT, etc, are composed of transistors, and the functions of digital gates are derived from the individual ON-OFF states of the transistors inside the gate, we know the basic unit of electronic devices is actually the transistors inside the IC. A good analogy is that atoms are the basic elements of all the materials.

If we want to reduce the power of a mobile device, one crucial step is to reduce the power of the IC inside the device. As mentioned above, reducing the power of each transistor is equivalent to the power reduction of the chip. In this paper, we will give a brief description of one digital gate, NOT gate (or inverter), as an example at first. Then several NOT gates will be concatenated as a test circuit for simulation and analysis. In the following sections, the simulation procedures will be introduced, and derived data are also presented. In the final section, We conclude the results of the data analysis. The optimal voltage which gives the balanced performance (ON-OFF switch speed) and power is proposed.

2. Background of NOT Gate

NOT gate, also called inverter, is used to build our test circuits. Fig. 1 is the structure of a NOT gate composed of two transistors, the top one is a P-MOS transistor, and the bottom one is a N-MOS transistor.

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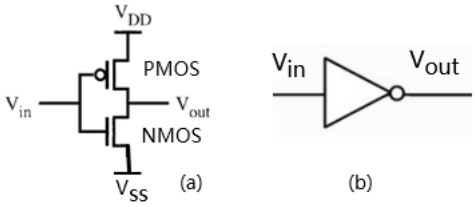

Figure 1: (a) The structure, and (b) the symbol, of a NOT gate.

The function of a NOT gate is described as below:

(1)VDD is the operating voltage. It depends on the technology of the semiconductor foundry. The foundry will give the recommended VDD, or nominal VDD, when a new technology is developed. Some examples are : (i) 1.10V is recommended for 40 nano-meter (nm) semiconductor technology by most of the foundries [4] (ii) 0.90V for 28nm technology. VSS is ground with voltage = 0.00V.

(2)If Vin = VDD (in the terminology of digital circuits, it is also called Vin = 1 or high), then PMOS is OFF and NMOS is ON. We can imagine that PMOS is like an open circuits, and NMOS is like a short circuits now. This leads Vout close to 0.00V. In digital circuits, it is called Vout = 0 or low.

(3)If Vin = 0.0V (Vin=0 or low), then PMOS is ON and NMOS is OFF. In this condition, PMOS is like a short circuits, and NMOS is like an open circuits now. This leads Vout close to VDD, Vout = 1 or high.

(4)Power consumption: theoretically, the power is consumed only during the ON-OFF switch, e.g., Vout changes to 1 from 0, or to 0 from 1. This power is proportional to (VDD)2. The details will be explained in the later section. This tells us that reducing VDD is directly related to the power reduction. This is our major theorem in this experiment.

(5)Performance: Lowering VDD will inevitably lower the output current, and the driving current from Vout to the Vin of the next gate becomes smaller. We can consider the next gate as a capacitor loading, since the current is smaller, it takes longer time to charge the capacitor to VDD (0-to-1) or discharge the capacitor to VSS （1-to-0). So, this lower VDD will make the speed of 1-to-0 or 0-to-1 slower. This switching speed is proportional the performance of the circuits. The details will also be explained in the later section.

With NOT gate, we can build our test circuits to investigate the optimal voltage for both power and performance.

3. Circuits Design

Our purpose is to build a circuits to measure its power consumption and switch speed through simulation. One usual way is to build a gate chain and calculate the average value of one gate. This is an industrial-level task beyond the high school scope. In our Microelectronics Club, one IC design house sponsored this project as practical training, and provided the design environment to us. This project is instructed by one engineering tutor with detailed document for our easy understanding.

The semiconductor technology, or semiconductor process, we adopted for this project is a nano-meter(nm)-level technology with faster speed and less power than micrometer (mm)-level technologies. Its nominal voltage for VDD is 0.85V. The tool used to design and simulate the circuits is Cadence Virtuoso[5].

The first step is to design a NOT gate with the provided PMOS and NMOS by the foundry, then we include the circuits into the NOT gate symbol as shown in Fig. 1. The second step is to concatenate 10 identical NOT gate serially given in Fig. 2 which is taken from Virtuoso.

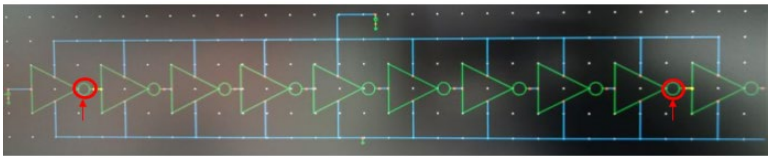

Fig. 2: Ten NOT gates are concatenated as the test circuits.

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4. Explanation for Power Consumption

Before doing the analysis and simulation, it is necessary to give a detailed description about the power consumption of these NOT gates in the chain as the inputs changes between 0-to-1 and 1-to-0. Fig. 3 is an example to tell where the power is consumed during the 0-to-1 and 1-to-0 change.

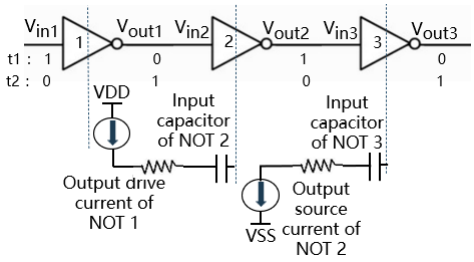

Fig. 3: Every NOT gate can be treated as an equivalent input capacitor and output current, here the resistor represents the resistance in the path from Vout to the next Vin.

Every logic gate, not only NOT gate, can be simplified as a model with an input capacitor and output current. This simplified model can help us in understanding the power consumption.

From Fig. 3, if Vout1 = Vin2 = 0 is changed to 1 (due to the change of Vin1, Vin1= 1 at t1, and is changed to 0 at t2), then the PMOS (which is connected to VDD) of NOT 1 is ON after t2, and the current from VDD is charged into the input capacitor of NOT 2, so the input of NOT 2 will be charged to 1 from 0, i.e. from low to high.

Also, after the input of NOT 2 is charged to high, the NMOS (which is connected to the ground, VSS) of NOT 2 is ON. Then the input capacitor of NOT 3 is connected to VSS, i.e., the input of NOT 3 is discharged from 1 to 0.

From the above description, we derived the conclusion:

(1)The power consumed in the NOT-gate chain is caused by the state change (0-to-1 and 1-to-0) of each NOT gate.

(2)Between two NOT gates, if it is 0-to-1, then the drive current from VDD charges the input capacitor to high.

(3)Between two NOT gates, if it is 1-to-0, then the source current discharges the input capacitor to the ground VSS.

(4)From [1], Chapter 23, we know the power of RCL circuits is P = I2Z or V2/Z, where Z is the impedance by R and C (input capacitor) in Fig. 3. Here I is the sum of the charging and discharging current between gates. Since the Z in the circuits is fixed (R and C will not be changed by operating voltage), the power consumption is proportional to I2 and V2. This is the explanation to the description in the previous section.

5. Explanation for Speed and Propagation Delay

For the simulation, we make the following measurements and calculation:

(1)Instead of simulating the power consumption in this circuits, we used (VDD)2 directly because we just want to have the power-to-performance ratio which will be explained later. No detailed valued of R and C is needed as in Fig. 3.

(2)Speed is the reciprocal of propagation time (see later). Checking Fig. 2, we will measure the propagation time from the left red circle to the right red circle. The details are explained below.

For each NOT gate, if Vin is changed from 0 to 1 at time t= t1, then Vout will be changed from 1 to 0 at t= t1 + Dt, where Dt is called propagation delay of this NOT gate. The propagation delay is explained in Fig. 4, which follows Fig. 3 with the explanation in the aspect of timing.

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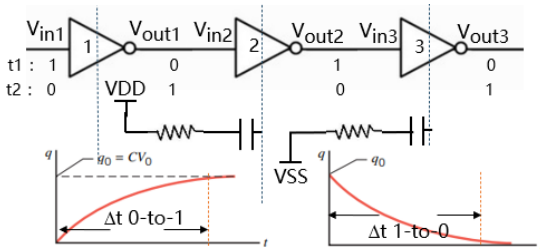

Fig. 4: The propagation delay caused by the charging and discharging time between gates.

From [1], Chapter 20, we learned the timing curve of charging or discharging the RC circuits. The timing constant t = RC determines the charging and discharging time. It is easy to understand that: in the NOT-gate chain of Fig. 2, the state change of Vout of each gate can not happens in the same time. After Vin2 is charged to 1 with Dt 0-to-1, then the NMOS in NOT 2 can be ON, then Vin3 can be discharged to 0 with Dt 1-to-0, and so on. This tells that the state change of Vout of each gate happens sequentially, from the first Vout1 to the last Vout, one by one. Each NPT gate needs a propagation delay of either Dt 0-to-1 or Dt 1-to-0 to change its state.

The shorter Dt is (no matter Dt 1-to-0 or Dt 0-to-1), the faster the gate reacts to the input change, and we say the better the performance is. From Fig. 2, we measure the propagation delay between the 8 NOT gates. The totally delay time is the sum of four Dt 1-to-0 plus four Dt 0-to-1 as shown in Fig. 5.

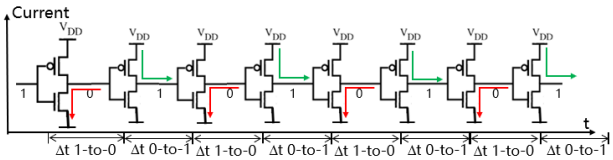

Fig. 5: The delay in the test circuits of Fig. 2.

In this figure, the red arrow line is the discharging current, its individual delay time is Dt 1-to-0. The green arrow line is the charging current, its individual delay time is Dt 0-to-1. Only the previous NOT gate is discharged and state is changed, then the following NOT gate can be charged, and vice versa. The more gates are concatenated in the chain, the longer total delay time is required.

6. Simulation Processes

We describe the details of simulation and measurement processes as below. Fig. 6 is the waveforms of the two red circles in Fig. 2, the X-axis is time, and the Y-axis is voltage.

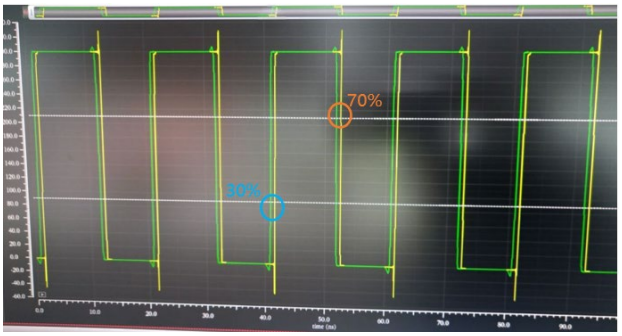

Fig. 6: The green waveform is the signal in the left red circle of Fig. 2, and the yellow waveform is the signal of the right red circle.

We can see there is a clear delay (time difference) between the two waveforms. The green waveform is the input signal to the 8 NOT gates as indicated by the left red circle in Fig. 2. The yellow waveform is the output signal from the 8 NOT gates as indicated by the right red circle in Fig. 2. It is obvious that the green waveform is leading the yellow waveform. The unit for the delay time is usually pico-second (ps), i.e., 10-12 second. In Fig. 6, for simplicity, we call the total Dt 0-to-1 through the eight NOT gates as the rising delay, and total Dt 1-to-0 through the eight NOT gates as the falling delay, in our later discussion.

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The rising delay is measured at the voltage indicated by the blue circle of Fig. 6, where the voltage rises to 30% position. The falling delay is measured as indicated by the orange circle, where the voltage falls to 70% position. There is no clear rule in the % definition, we can also measure both delay in 50% position. The only rule is to make a fair and fixed measurement in all the tested VDD.

With this test circuits and measurement method, we simulated different VDD to check the delay value.

7. Simulation Results

The nominal voltage of this semiconductor technology is 0.85V. In this project, we simulated the following 9 voltages : 0.95V, 085V, 0.75V, 0.65V, 0.55V, 0.45V, 0.35V, 0.30V, 0.25V. In order for the fair comparison, the test circuits is kept the same, and we also use the same temperature in all the simulation because the temperature will impact the speed and power consumption of transistors.

Table 1: Simulation data and analysis result

Voltage (V)	0.95	0.85	0.75	0.65	0.55	0.45	0.35	0.3	0.25
Power (= V^2)	0.903	0.723	0.563	0.423	0.303	0.203	0.123	0.09	0.063
Averaged Delay Time (pico-second)	42	45	51.5	65.5	90.5	142	329	743	2600
1/(Power * Delay) speed/power ratio	0.026	0.031	0.035	0.036	0.037	0.035	0.025	0.015	0.006

Table 1 is the data from simulation, and our analysis results is based on these data.

In Table 1,

(1)The 1st row: the 9 voltages we did for simulation individually.

(2)The 2nd row: the power consumption which is equal to V2.

(3)The 3rd row: the delay time which is measured from the simulation. Fig. 5 and Fig. 6 tell there are 2 types of delay time, the rising delay and the falling delay. The delay time is the average of these two delay time.

(4)The 4th row: the analysis data of speed/power ratio, explained as below.

We can find that the delay time increases (the 3rd row) as the power (the 2nd row) decreases. But the relation between the increase and decrease is not linear. One obvious example is V=0.95V and V=0.30V : even though the power consumption is 10 times smaller if we use V=0.30V compared with V=0.95V, the delay time is 743/42 = 17.7 times larger. So, V=0.30V is not a good choice no matter how low the power is due to the poor performance.

One index is adopted for evaluating the tradeoff of power and performance, it is called speed/power ratio (the 4th row) with the following equation:

$$\text{Speed/power ratio} = \frac{1}{\text{power} * \text{delay time}}$$

The ON-OFF switching speed is the reciprocal of delay time. Since the power is in the denominator of this index, the higher the index is, the better performance it can reach based on the same power consumption. We can see V=0.55V can achieve the best ratio among the 9 voltages, as shown in Fig. 7.

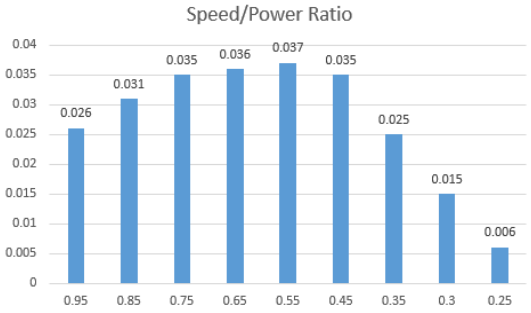

Fig. 7: The plot of speed/power ratio in Table 1. The x-axis is the operating voltage, and the Y-axis is the ratio.

In this figure, it is clear that 0.55V gives the highest ratio. We can translate the meaning in a

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simpler statement: if the power consumption is fixed, then we can have the best performance with VDD = 0.55V. This is the optimal point we are looking for in this semiconductor technology.

It is reasonable to select the 0.55V as the operating voltage in our design. But it is not always true for some other applications. We will check two different examples.

The first example is the application which emphasizes speed more than power saving. This application can sacrifice the power to keep a higher speed. In this case, the ratio will be different from that in Table 1 and Fig. 7. Since we emphasize speed, this is equivalent to deemphasizing the delay time. One possible way is to use the equation as below:

$$\text{Speed/power ratio} = \frac{1}{\text{power} * (\text{delay time})^2}$$

The delay time is in the denominator, its square can deemphasize its importance if it is getting larger. With this new equation, the new ratio which emphasizes performance is given in Fig. 8.

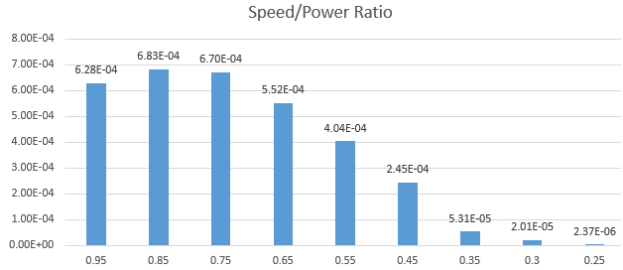

Fig. 8: The plot of speed/power ratio in emphasizing the performance.

We can see VDD = 0.85V is recommended by the option. Of course the equation for this performance/power ratio is one choice only, there can be some other ways to define this ratio equation to emphasize performance.

The second example is the application which emphasizes power saving more than speed. This application can sacrifice the speed to keep the power as low as possible. In this case, the ratio will also be different from that in Fig. 7 and Fig. 8. One possible way is to use the equation as below:

$$\text{Speed/power ratio} = \frac{1}{(\text{power})^2 * \text{delay time}}$$

Even though the power is in the denominator, its value is smaller than 1.0, and its square value will be even smaller, then the ratio will be larger. This can emphasize its importance. With this new equation, the new ratio which emphasizes power is given in Fig. 9.

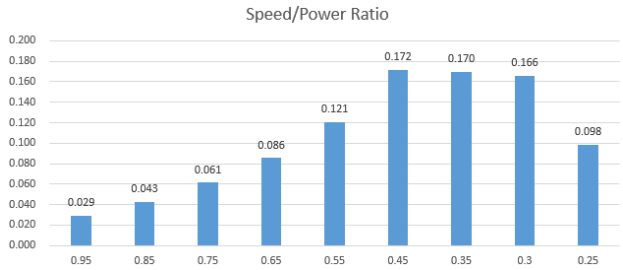

Fig. 9: The plot of speed/power ratio in emphasizing the power.

We can see VDD = 0.45V is recommended by the option. Also the equation for this performance/power ratio can be in some other ways to emphasize power.

8. Conclusion

From the above analysis, V=0.55V is proposed as the operating voltage for this semiconductor technology because this voltage gives the best speed/power ratio without specially emphasizing either power or speed. For some portable devices such as Bluetooth earphone, even its IC emphasizes power consumption more than speed, its performance is still required to be in several hundred mega-hertz (MHz), we still need to keep a certain moderate performance. In this application case, VDD=0.55V is a good choice for this design and operation, it gives much lower power than 0.85V but still keep the

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performance as it required. The sponsoring IC design company adopts this results in the real design work. It is our major achievement in this project.

For the IC in cellphone such as application processor which requires performance of giga-hertz (GHz) level, its choice will be 0.85V instead of 0.55V because performance is the key requirement. 0.55V can not reach GHz-level performance. That is why the nominal voltage is 0.85V proposed by the semiconductor foundry because the first product of a new advanced technology is usually cellphone IC.

For the IC such as used in the smoke detector inside the buildings, it is operated in a very low speed, but it requires an extremely low power. Since it is supplied by battery, and it is not convenient to change the battery often, it must be low power. In this application, 0.45V ~ 0.35V may be a good operating voltage.

This evaluation method we learned from this project can be applied to all the semiconductor technologies. Each technology gives different characteristics in performance and power. This method is simple and straightforward, it is helpful in finding the optimal point.

Different voltage gives different results, the designers should choose the one which fits the application the best from consideration in both power and performance.

Acknowledgement

This project is sponsored by one IC design house which required to be anonymous in this paper. Besides the instructor and his teaching in our Microelectronics Club, the company also provided the simulation tool and necessary technology information during the period of our practical training. We verified the basic knowledge in our physics class through this project, we also learned new techniques through the circuits design and simulation. We derive much more than what we contributed to this company.

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