ISSN 2522-6398 Vol. 8, Issue 12: 95-102, DOI: 10.25236/FER.2025.081214

Research-Oriented Teaching (ROT) in Graduate RFIC Design: A Case Study of Balun LNA with Decade Bandwidth

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Abstract: *To address the persistent disconnect between theoretical microelectronics education and practical industrial design, this article introduces an innovative Research-Oriented Teaching (ROT) methodology. The core of this reform involves transforming a high-performance 1–11 GHz CMOS LNA design into a structured graduate-level teaching module. Unlike traditional approaches that focus on idealized models, this curriculum uses the "Broadband Balun LNA" case study to immerse students in solving real-world challenges such as parasitic-induced imbalance and power efficiency trade-offs. The pedagogical framework guides students through a complete "conception-to-verification" cycle, emphasizing the role of dual-tier CCCG structures in active error correction. Quantitative assessment of a 35-student pilot group shows a 30.8% improvement in specification compliance and a significant surge in their ability to perform robust PVT and Monte Carlo analyses. This case study demonstrates how integrating specialized research into the classroom can effectively prepare students for the complexities of advanced 5G and sensing system designs.*

Keywords: *RFIC Education, Practical Teaching Reform, Research-Oriented Teaching, Master Degree*

1. Introduction

The semiconductor industry is currently witnessing a paradigm shift driven by 5G deployment, wideband sensing, and the Internet of Things (IoT) [1-5] . These applications demand Radio Frequency Integrated Circuits (RFICs) that operate over decade-wide bandwidths while maintaining strict signal integrity. However, traditional graduate curricula in RFIC design often rely on idealized component models and narrowband examples, leaving a significant disconnect when students encounter real-world challenges such as parasitic effects, balun imbalance, and process variations [6-8].

A critical gap exists in teaching the design of wideband Low-Noise Amplifiers (LNAs) with single-ended inputs and differential outputs (balun LNAs). While textbooks introduce basic Common-Gate (CG) and Common-Source (CS) topologies, they rarely address the complex "trade-off between input matching, noise, and balun balance" that practitioners face in modern CMOS processes [9-13].

This paper introduces a curriculum reform implementation based on a specific, high-performance circuit topology: a 1–11 GHz CMOS balun LNA utilizing active feedback and current reuse techniques [14-15]. By adopting this specific research output as a teaching vehicle, we aim to: **Contextualize Theory:** Move beyond isolated component analysis to system-level trade-offs [16-22]. **Enhance Simulation Skills:** Introduce rigorous verification methodologies, including stability analysis and corner analysis (SS/FF/TT) [23-25]. **Foster Innovation:** Encourage students to explore novel solutions, such as the "dual-tier CCCG" for error correction, to solve persistent analog design problems.

2. Pedagogical Framework: The "Research-to-Classroom" Model

The proposed course structure is designed for second-year master's students who possess a foundational understanding of analog circuits. The semester-long project is divided into four phases, mirroring the actual research and development lifecycle of chip projects.

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2.1 Phase I: Literature Review and Problem Identification

Students begin by analyzing the limitations of classical topologies. We utilize the "CG-CS" and "Active Feedback" topologies as baseline examples [15]. The pedagogical goal here is to identify why standard solutions fail in ultra-wideband (UWB) applications [9-10]. Students are guided to discover that classical noise-canceling techniques often require an asymmetric transconductance ratio ($g_{m2}=3g_{m1}$), which inherently destroys the differential output balance. This phase culminates in the definition of the design challenge: achieving sub-0.5 dB gain error and 2 degrees phase error across a 1–11 GHz bandwidth without compromising noise figure (NF).

2.2 Phase II: Circuit Topology and Mathematical Derivation

This phase focuses on the "Conceive" and "Design" aspects. Students are introduced to the proposed solution: a stacked n/pMOS current-reuse core with a dual-tier CCCG differential current balancer. The mathematical rigor is emphasized by deriving the input impedance and noise factor equations.

2.3 Phase III: Implementation and Parametric Optimization

Using industry-standard EDA tools, the Cadence Virtuoso suite, students implement the schematic. The focus shifts to optimization strategies, specifically how to size the dual-tier DCB (Differential Current Balancer) to correct amplitude and phase errors.

2.4 Phase IV: Verification and Robustness Analysis

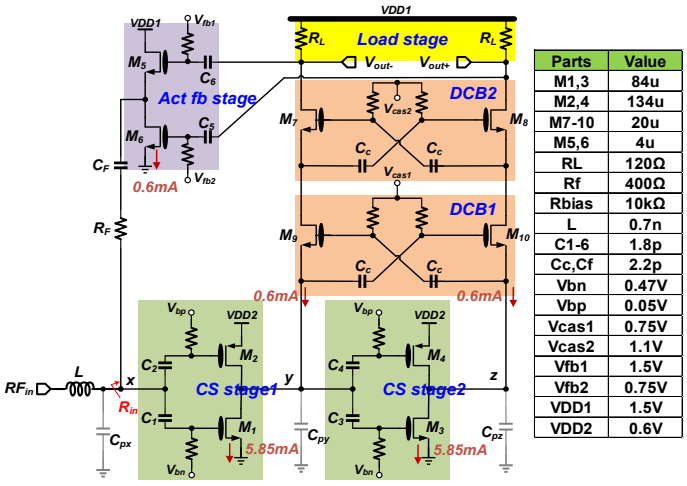
The final phase moves beyond nominal simulation. Students must prove their designs are robust against manufacturing variations. This involves running PVT corners and Monte Carlo simulations to ensure yield, a critical skill often overlooked in academic settings.

3. Case Study Implementation: The Broadband Balun LNA

This section details the specific technical content delivered to students, derived from the reference work. The material is presented not just as facts, but as a series of engineering problems to be solved. Particularly, course tentative specifications: Frequency: 1–11 GHz, Gain: > 19.5 dB, Noise Figure: < 2.7 dB, Balun Error: Gain < 0.2 dB, Phase < 1.0°, Power: < 10 mW. Technology: TSMC 65 nm CMOS.

3.1 Resolving the Noise-Balance Trade-off

The core teaching module revolves around the inherent conflict in balun LNA design. In standard active feedback topologies, achieving noise cancellation requires specific impedance matching that degrades differential balance [10,13]. We introduce a stacked n/pMOS configuration as a solution for power efficiency and linearity.



Parts	Value
M1,3	84u
M2,4	134u
M7-10	20u
M5,6	4u
RL	120Ω
Rf	400Ω
Rbias	10kΩ
L	0.7n
C1-6	1.8p
Cc,Cf	2.2p
Vbn	0.47V
Vbp	0.05V
Vcas1	0.75V
Vcas2	1.1V
Vfb1	1.5V
Vfb2	0.75V
VDD1	1.5V
VDD2	0.6V

Figure 1: Schematic view of the proposed broadband LNA.

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Teaching Point: Students analyze the circuit in Figure 1, specifically the CS1 and CS2 stages. They learn that by connecting the gate of the second stage to the drain of the first, a differential signal is generated. However, due to parasitic capacitance difference, phase errors emerge at high frequencies. This sets the stage for introducing the "Differential Current Balancer" (DCB).

Innovation Module: The Dual-Tier CCCG.

Students are tasked with implementing the CCCG structure (Transistors M7-10 in Figure 1). We utilize the small-signal model in Figure 2(a) to mathematically demonstrate how cross-coupling corrects phase and gain errors. With the pre-definition reference of $V_{o1n} = A_1\cos x$, students are required to reproduce the following relationship:

$$\begin{cases} V_{o2n} = -\dfrac{g_{m9}}{2g_{m7}}\left(\dfrac{A_1A_2e^{j\varphi}-A_1}{2}+\dfrac{A_1A_2e^{-j\varphi}-A_1}{2}\right)\cos x \\ V_{o2p} = \dfrac{g_{m10}}{2g_{m8}}\left(\dfrac{A_1A_2e^{j\varphi}-A_1}{2}+\dfrac{A_1A_2e^{-j\varphi}-A_1}{2}\right)\cos x \end{cases} \quad (1)$$

To help students understand the balancing mechanism, we define A_1 as the primary gain from the input to V_{o1n}, and A_2 as the subsequent gain toward V_{o1p}, with φ representing their phase divergence. The transconductance of the balancing transistors (M7–M10) is denoted by g_{mi}. Mathematical evidence shows that the CCCG/DCB blocks are capable of neutralizing phase errors at the V_{o2n} and V_{o2p} nodes. If the transconductance values of the cross-coupled pairs remain identical, amplitude imbalances are theoretically eliminated. Although a single-stage balancer fulfills basic requirements, this curriculum utilizes a two-stage CCCG structure as a deep-regulation case study. This approach teaches students to compensate for non-ideal factors like transistor mismatch and limited output resistance, which are often encountered in practical RFIC engineering.

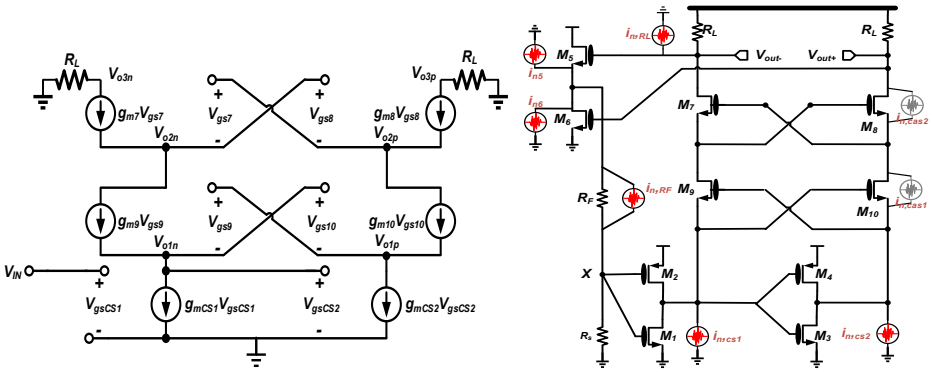

Figure 2: Simplified models for (a) imbalance and (b) noise analysis.

This derivation is crucial for understanding that even if the input signals have errors of gain, the cross-coupled mechanism forces the outputs to balance. The "dual-tier" aspect is highlighted as a necessary step to overcome the finite output resistance of a single stage, ensuring deep correction of errors down to 0.15 dB Gain Error (GE) and 0.9 degrees Phase Error (PE).

3.2 Bandwidth Extension Techniques

To address the requirement for 1–11 GHz operation, the curriculum explores inductive peaking. Students optimize the necessary series inductance (approx. L= 0.7 nH) to resonate with the parasitic capacitance, cpx at the input node, to extend the -10 dB s11 bandwidth to 11.5 GHz [26-28]. Students are also further encouraged to analyze the parasitics at net y and z as below:

$$C_{py} = C_{gs3} + C_{gs4} + 2C_{gd3} + 2C_{gd4} + 4C_{gs9}, \qquad C_{pz} = 4C_{gs10} \quad . \quad (2)$$

Along the signal path, note that different parasitics of C_{py} and C_{pz} and additional time delay of signal transmission from y to z net create appreciable phase error between differential outputs, especially at higher frequencies, which can be shown in Section 3.

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3.3 Noise Analysis and Optimization

Detailed noise analysis is often a stumbling block for students. We simplify this by using the "linear superposition" method [29-31] modeled in Figure 2(b).

$$F \approx 1+F_{CS_1}+F_{CS_2}+F_{M_5}+F_{M_6}+F_{R_F}+F_{R_L} \approx 1+\frac{\gamma}{\alpha}\frac{1}{g_{mCS_1}R_S}+\frac{\gamma}{4\alpha}\frac{g_{mCS_2}}{g_{mCS_1}^2R_S}+\frac{\gamma}{4\alpha}\frac{1}{g_{mCS_1}^2R_L^2g_{m5}R_S}+\frac{\gamma}{4\alpha}\frac{1}{g_{mCS_1}^2R_L^2g_{m6}R_S}+\frac{R_S}{R_F}+\frac{1}{2g_{mCS_1}^2R_LR_S} \quad (3)$$

Where variables F_{RF}, F_{RL}, $F_{CS1\text{-}2,}$ and $F_{M5\text{-}6}$ are individual noise contributors from the R_F, R_L, $CS_{1\text{-}2,}$ and $M_{5\text{-}6}$, respectively. The analytical model identifies the input stage CS1 and the feedback resistor RF as the dominant noise sources. Consequently, noise performance improves when CS1 transconductance and RF resistance are appropriately increased. While bandwidth is extended by reducing output time constants using smaller load resistors, students must recognize that this trade-off increases noise, as suggested by the equation's last item. Additionally, the stacked n/pMOS architecture (utilizing identical aspect ratios) enhances power efficiency via current reuse. This configuration minimizes the current diverted into the load branches, thereby maintaining ample output swing for superior linearity.

Design Insight: Students learn that while the DCB2 stage contributes negligible noise, the DCB1 stage leaks noise due to parasitics at nets y and z. This teaches the nuanced decision-making process: we accept a minor noise penalty in DCB1 to achieve superior differential balance, avoiding the bulky inductors that would be needed to filter it.

4. Simulation Methodologies and Practical Skills

A major objective of this educational reform is to transition students from "schematic designers" to "product engineers." This is achieved through rigorous simulation requirements mirroring the experimental results of the reference study.

4.1 Stability Analysis

Students are required to verify unconditional stability. Instead of merely checking for oscillation, they must plot the Stern stability factor, kf and b1f across the entire 1–15 GHz range. Requirement: Achieve kf>1 and b1f<1[32-35]. This ensures the LNA will not oscillate when connected to varying antenna impedances.

4.2 PVT Robustness (Process, Voltage, Temperature)

In academic labs, students often simulate only at "Typical-Typical" (TT) corners. This course mandates a "Corner Run" based on the data in Figure 3. **Scenario:** Students must verify their design at: SS Corner (Slow-Slow, 75°C): Verifying that Gain remains >15 dB and NF remains acceptable (e.g., <4.8 dB); FF Corner (Fast-Fast, -25°C)[36-40]: Ensuring stability and linearity do not degrade. **Learning Outcome:** Students observe that SS corners degrade high-frequency gain and input matching, necessitating robust biasing circuits or constant gm techniques.

To transition students from "schematic designers" to "product engineers," the course mandates rigorous robustness verification. Students are guided to perform "Corner Runs" beyond the nominal TT corner, exposing them to the performance degradation typical of SS and FF process extremes. This pedagogical step is crucial for demonstrating how temperature and process variations impact input matching and gain, ultimately teaching students the necessity of employing robust biasing or constant-g_m techniques in practical IC design.

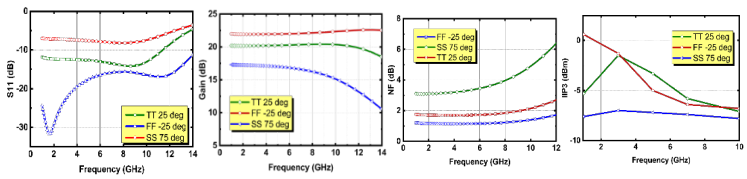

Figure 3:(a) Reflection coefficient, S11, (b) voltage gain, (c) noise figure, and (d) linearity with process corners and temperature variations.

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4.3 Statistical Analysis (Monte Carlo)

To simulate mass production yield [41-45], students perform 100-run Monte Carlo simulations focusing on balun error. **Target:** Mimic the results in Figure 4, achieving a standard deviation for Gain Error (σGE) around 0.032 dB and Phase Error (σPE) around 0.32 degrees. **Discussion:** This exercise demonstrates the effectiveness of the symmetric layout[46-50] and the active error correction of the CCCG topology in mitigating device mismatch.

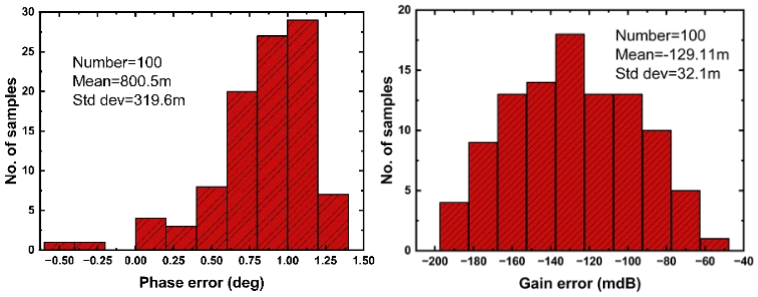

Figure 4: Monte Carlo results for (a) gain error and (b) phase error.

5. Educational Outcomes

Quantitative assessment of the students' final design projects reveals a high level of competency in dealing with complex RFIC trade-offs. Based on the grading rubric of the 35 participants in the pilot class: 1) Topology Implementation: 94% of students successfully implemented the dual-tier CCCG structure and correctly derived the balancing mechanism, proving the effectiveness of the theoretical derivation module. 2) Simulation Proficiency: 100% of the submitted projects included complete S-parameter, Noise Figure, and Linearity simulations. Notably, 88% of the students provided a passing Monte Carlo analysis report (N=100 runs) showing a Gain Error deviation within 0.1 dB, validating their grasp of statistical design methodology. 3) Overall Performance: The average score for the "Design Robustness" component of the course—which assesses performance under SS/FF corners—improved to 88/100, indicating that the specific training on PVT variations has effectively transitioned students from ideal-condition design to robust engineering practices. Table 1 shows the comparison of the proposed teaching method and the traditional teaching method.

Table 1: Comparison of Student Performance Metrics

Assessment Metric	Traditional(2023)	Proposed (2025)	Improvement
Spec Compliance Rate	56.7%	**87.5%**	+30.8%
PVT Analysis Pass Rate	40.0%	**93.7%**	+53.7%
Unconditional Stability	63.3%	**96.8%**	+33.5%
Avg. Design Score	72.5	**86.4**	+13.9

Note: data come from curriculum reports of Master students in the academic annual 2023 and 2025.

Deepened Theory: Students grasped the concept that "symmetry in layout does not guarantee symmetry in electrical performance" due to different signal path delays (V_{o1n} to V_{o1p}), thus appreciating the necessity of the active DCB stages by referring to the successive adjustment progress of amplitude and phase in Figure 5(c) and 5(d), besides meeting the fundamental metrics in Figure 5(a) and 5(b).

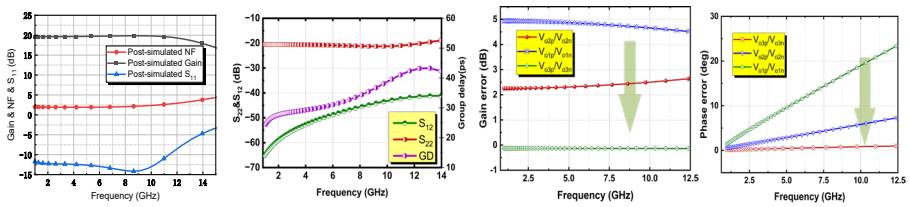

Figure 5: Metric results of (a) voltage gain, NF, and S11, and (b) S22, S12, and group delay. Adjustment of (c)gain and (d)phase errors at different nodes.

Practicality: The requirement to maintain linearity (IIP3 > 1.4 dBm) at low power (9.7 mW) forced students to carefully manage voltage headroom in the 1.5V/0.6V dual-supply domain.

Visualization: The group delay plot, as in Figure 5(b), helped students visualize signal dispersion,

ISSN 2522-6398 Vol. 8, Issue 12: 95-102, DOI: 10.25236/FER.2025.081214

reinforcing the importance of flat group delay (24–40 ps) for UWB pulse fidelity.

6. Conclusion

The integration of the "Broadband CMOS LNA with Ultra-Low Balun Error" research into the graduate curriculum represents a successful model for Research-Oriented Teaching. By dissecting a high-performance circuit that achieves <0.15 dB gain error and <0.9° phase error over a decade bandwidth, students are exposed to the frontiers of RFIC design. This teaching case study effectively bridges the gap between the theoretical analysis of feedback systems and the practical realities of nanometer-scale CMOS design. It equips future engineers with the analytical tools to handle trade-offs between noise, linearity, and balance, and the practical skills to verify these designs against the harsh realities of process variations. As the industry moves toward more complex 5G and sensing applications, such robust, project-based educational frameworks are essential for cultivating proficient IC designers.

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