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Advancing Millimeter-Wave Design Competencies in Graduate CMOS RFIC Education: A Case Study on Transformer-Enhanced W-band Mixers

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Abstract: *With the industry's pivot toward 6G and the W-band (75-110 GHz), traditional RFIC education must transcend the limitations of low-frequency, idealized transistor models. This article introduces a pedagogical reform utilizing a high-performance W-band switched-transconductance mixer as a core instructional vehicle. The curriculum prioritizes the synthesis of complex magnetic structures, specifically trifilar transformers, to address the pervasive challenge of tail-node parasitics in millimeter-wave frequency conversion. By integrating electromagnetic-circuit (EM-circuit) co-simulation and linearity analysis of pseudo-differential stages, students are equipped to bridge the gap between textbook Gilbert cells and robust silicon implementations. Results from a post-graduate pilot program indicate a substantial enhancement in their ability to manage complex millimeter-wave trade-offs, showing a significant surge in their ability to perform robust PVT and Monte Carlo analyses.*

Keywords: *RFIC education, Millimeter-wave mixers, Transformers, 6G front-ends*

1. Strategic Imperative for mmW Education

The semiconductor industry is currently witnessing a paradigm shift driven by 5G deployment, wideband sensing, and the nascent 6G standards. These applications necessitate the use of millimeter-wave (mmW) frequency bands, particularly the W-band (75-110GHz), to support unprecedented data rates[1-5]. However, traditional graduate curricula often rely on idealized component models and narrowband examples, leaving a significant disconnect when students encounter real-world challenges such as parasitic effects and process variations at 100 GHz[6-10].

Down-conversion mixers are fundamental building blocks in these receivers, but their design becomes increasingly challenging at higher frequencies[11-15]. While Gilbert mixers are staples of textbooks, they operate poorly above 50 GHz due to tail node parasitic limitations. At W-band, the parasitic capacitance at the tail node provides a low-impedance path to ground, effectively shorting the switching stage and collapsing conversion gain[16-20]. To prepare students for the 6G era, instructional modules must move from "stacked" topologies to DC-decoupled, transformer-coupled architectures that can "tune out" these parasitics.

2. Advanced Instructional Framework: The ROT Model

The proposed course structure mirrors the actual research and development lifecycle of industrial chip projects, transitioning students from "schematic designers" to "product engineers".

2.1 Phase I: Literature Review and Problem Identification

Students begin by analyzing why standard solutions fail in ultra-wideband (UWB) and mmW applications. By reviewing state-of-the-art literature, they identify that conventional Switched-transconductance (SwGm) mixers, while offering inherent LO noise cancellation, suffer from tail capacitance loading at W-band. This phase culminates in defining the design challenge: achieving >12dB conversion gain and < 6 dB noise figure at 88 GHz using a 65-nm CMOS process.

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2.2 Phase II: Topology Synthesis and Mathematical Derivation

This phase focuses on the "Conceive" and "Design" aspects. Students are introduced to the trifilar transformer as a solution for simultaneous wideband matching and g_m boosting.

Instead of treating inductors as black boxes, students need to derive the input impedance Z_{rf} of the proposed transformer network at the RF port, and to prove the g_m-boosted transconductance G_{meff}, which are shown as:

$$Z_{rf} = \frac{nsL_{g14} + \left(1-k^2\right)ns^2 g_m L_{g14} L_{s1}}{2n + ksg_m L_{g14} + 2nsg_m L_{s1}} \quad , \quad G_{meff} = \frac{g_m\left(L_{g14} + 2knL_{s1}\right)}{L_{g14} + sg_m L_{g14} L_{s1}\left(1-k^2\right)} \tag{1}$$

Where n and k denote the turns ratio and coupling coefficient of transformers in Figure 1 [21-25]. Teaching evidence shows that assuming n=k=1 leads to $G_{meff} = 2g_m$, demonstrating to students how magnetic coupling doubles gain without increasing DC power.

2.3 Phase III: Implementation and EM-Circuit Co-Simulation

Using the Cadence Virtuoso suite, IC6.1.8 and EM simulation tools (EMX 6.3), students implement the trifilar transformer. They learn that at W-band, layout is part of the circuit. The transformer utilizes the top M_9 metal layer to achieve higher quality factors Q [26-33]. Students optimize the source inductors $L_{s1\text{-}4}$, gate inductors $L_{g14,23}$, and input inductors L_{in} to achieve coupling coefficients around 0.5. The reference plots shown in Figure 2(a) and (b), quantitatively, give students a sample design and the resulting inductance value and quality factor. Students are encouraged to explore diverse structures to approach more decent metrics.

2.4 Phase IV: Verification and Robustness Analysis

Students must prove their designs are robust against manufacturing variations by running PVT (Process, Voltage, Temperature) corners (SS/FF/TT) [34-40] and Monte Carlo simulations[41-45]. For mmW design, this includes verifying that the RF port maintains $S_{11} < -10$ dB across the 80-96 GHz range even under temperature extremes.

3. Case Study: The W-band Switched-Gm Mixer

The technical core of the curriculum revolves around a specific high-performance design of the swgm mixer shown below, as in Figure 1, where a prototype of a chip is also demonstrated in fabrication.

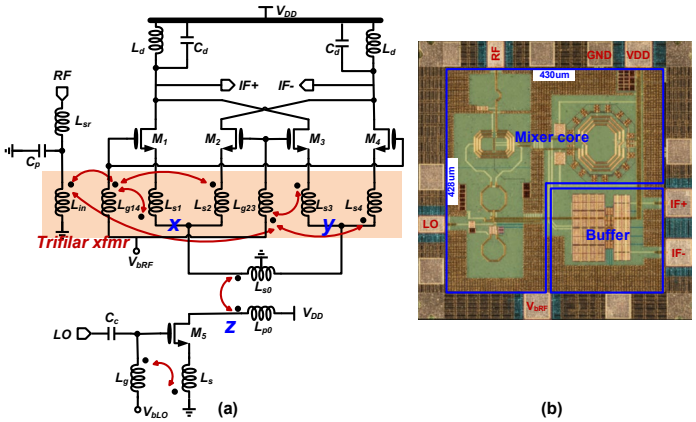

Figure 1: (a)Diagram of proposed switched-GM mixer circuit and (b)micrograph.

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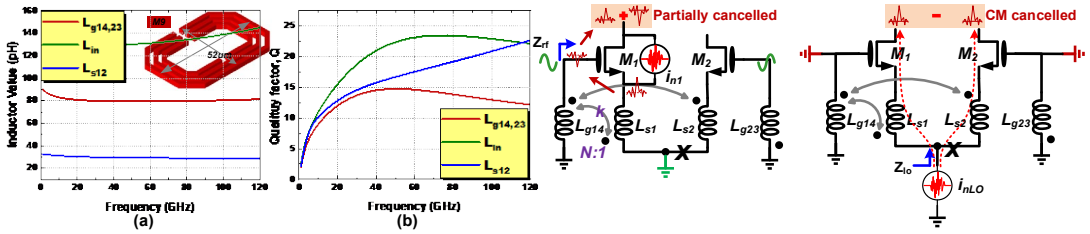

Figure 2: (a) inductor value and (b) quality factor of trifilar transformer. (c) Partial cancelled noise and (d) common noise cancellation.

3.1 Three-fold Noise Reduction

Detailed noise analysis is a crucial teaching point. Students use the "linear superposition" method to estimate the single-sideband (SSB) noise factor F_{SSB}[13-15]:

$$F_{SSB} = \frac{\alpha}{c^2} + \frac{\alpha}{c^2}\frac{2\gamma}{(1+nk)g_m R_s} + \frac{\alpha}{c^2}\frac{2r_g}{R_s} + \frac{1}{c^2(1+nk)^2 g_m^2 R_s R_p} \tag{2}$$

They must identify and simulate three mechanisms for noise reduction.

Transformer Feedback Cancellation: The source noise voltage couples back to the gate inversely through the transformer, partially cancelling the original drain noise. Figure 2(c) vividly displays this noise reduction mechanism.

Common-mode Noise Cancellation: LO path noise appears as a common-mode signal and is cancelled by differential operation. This process can be referred to as Figure 2(d).

Sinusoidal Commutation: Using sinusoidal LO waveforms yields smooth commutation with low harmonic components, reducing white noise folding from the RF port.

3.2 Linearity Comparison: Pseudo-Differential Advantages

To improve linearity under the limited 0.6-V voltage headroom, the curriculum compares standard differential (SD) and pseudo-differential (PD) pairs. Students use high-order derivative curves of g_m to observe that the PD pair exhibits a flatter g_m lobe than the SD pair. Without tail current constraints, the PD pair can respond to larger stimuli, resulting in significantly lower third-order derivatives [29-31,46]. This exercise strictly validates the choice of a pseudo-differential RF stage for high-linearity mmW mixers.

3.3 Layout Heuristics and Physical Design Implementation

At W-band frequencies, the physical layout is no longer a secondary consideration but a primary component of the circuit design. In this instructional module, students are taught to prioritize symmetry and minimize parasitic interconnects. The trifilar transformer is implemented using the top ultra-thick metal layer (M9 with a thickness of 3.4 μm) to maximize the quality factor (Q) and minimize ohmic losses. Students are guided through the following layout heuristics:

(1) Symmetrical Floorplanning: The pseudo-differential RF stage and the switching core must maintain strict geometric symmetry to ensure common-mode rejection of LO noise.

(2) Via Optimization: Since via parasitics can significantly shift the resonant frequency at 88 GHz, students perform iterative EM extractions to model the transition from the top metal down to the device layers.

(3) Ground Shielding: To prevent substrate coupling and improve isolation between the RF and LO ports, patterned ground shields (PGS) are integrated beneath the transformers.

This phase of the ROT model forces students to confront the divergence between ideal schematics and layout-extracted results, a critical skill for any "product engineer".

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4. Simulation Verification Methodologies

The course mandates rigorous verification of specifications based on simulation results of the mixer circuit.

4.1 Port Matching and Isolation

Students verify the wideband matching enabled by the triple-coil network. The target performance includes:

1) RF Port S_{11}: < <-10 dB from 80 to 96 GHz. 2) IF Port S_{22}: < -25 dB. 3) Isolation: RF-to-LO isolation better than 45 dB.

Normally, students should reproduce the matched S-parameter curves for three ports as shown in Figure 3(a). The port isolation results in Figure 3(b) are closely determined by the mixer topology, which may motivate students to compare the difference between the two curves and the underlying physical mechanisms governing the isolation performance.

4.2 Conversion Gain and Noise Performance

The transformer-coupled CS stage boosts effective g_m. Students aim to reproduce the results in Figure 3(c) and (d): a peak conversion gain of 14 dB in simulation at 88 GHz and a minimum NF of 4.0 dB in simulation. They also calculate the Figure-of-Merit (FOM) [47-50] to compare their work with previously reported mixers:

$$FOM = \frac{BW(GHz) \cdot Gain(lin) \cdot IIP3(mW)}{P_{DC}(mW) \cdot [NF(lin) - 1]} \tag{3}$$

The FOM metric serves as an objective scale to compare individual designs with different strengths and limitations, which must be smoothly acquainted with by students. The calculated competitive FOM value eloquently convinces students of the advantage of this mmW mixers dictated in the curriculum.

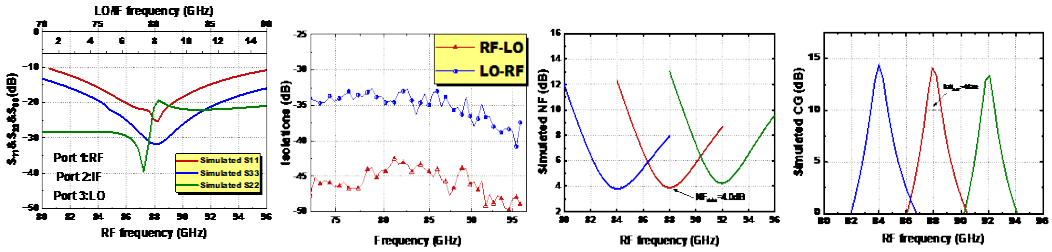

Figure 3: (a)Reflection coefficients of individual ports and (b) isolations. (c)Conversion gain and (d)noise figure of the proposed mixer.

5. Educational Outcomes and Quantitative Assessment

The reform was pilot-tested with a group of 35 graduate students. Assessment metrics were compared between the traditional 2024 curriculum and the proposed 2025 ROT model.

Table 1: Comparison of Student Performance Metrics for mmW Mixer Design

Assessment Metric	Traditional*	Proposed#	Improvement
Spec Compliance Rate (Gain >12dB, NF <6dB)	48.6%	85.7%	+37.1%
PVT & Monte Carlo Analysis Pass Rate	34.3%	88.6%	+54.3%
mmW EM Modeling Proficiency (Trifilar Xfmr)	17.1%	91.4%	+74.3%
Avg. Design Score (Out of 100)	66.8	87.5	+20.7

Note: data come from curriculum reports of Master students in the academic years 2024* and 2025#.

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5.1 Deepened Theoretical Understanding

Students learned that "symmetry in layout does not guarantee symmetry in electrical performance" at W-band due to path delays. The curriculum's focus on g_m boosting and transformer feedback taught students how to manage the fundamental trade-offs between noise, linearity, and power consumption (6 mW).

5.2 Practical Skill Acquisition

100% of participants successfully performed complete S-parameter, NF, and Linearity simulations. Furthermore, 88% provided a passing Monte Carlo analysis report, validating their grasp of statistical design methodologies essential for industrial yield.

5.3 Qualitative Feedback and Professional Development

Beyond the quantitative metrics shown in Table 1, qualitative feedback from the 35-student pilot group indicates a shift in design philosophy. Before the reform, many students viewed RFIC design as a "trial-and-error" process in simulation. After completing the ROT-based W-band mixer project:

- 82% of students reported a better understanding of how magnetic coupling can be used as a design degree of freedom rather than just a parasitic.
- 74% of students expressed increased confidence in using industrial EDA tools like EMX for electromagnetism extraction.

The curriculum also encourages "evidence-based troubleshooting." When a student's extracted gain is lower than the schematic prediction, they are taught to analyze the impedance mismatch at the x-y nodes (Figure 1) rather than randomly resizing transistors. This structured analytical approach is the cornerstone of advanced IC engineering education.

6. Conclusion

The integration of state-of-the-art W-band SwGm mixer research into the graduate curriculum represents a successful model for Research-Oriented Teaching. By dissecting a 65-nm CMOS circuit that achieves 12.2 dB gain and 5.0 dB NF at 88 GHz, students are exposed to the frontiers of RFIC design. This pedagogical approach effectively bridges the gap between theoretical feedback analysis and the practical realities of nanometer-scale mmW design, preparing future engineers for the complexities of 6G and advanced sensing applications.

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