

Research on high power and high efficiency DC/DC conversion power supply

Renbo Xu, Guihong Yu

School of Information and Artificial Intelligence, Nanchang Institute of Technology, Nanchang, 330108, China

Abstract: Buck-boost converter is widely used in semiconductor lighting control system. And in this paper, its operating mode and other characteristics are discussed, by using PID (Proportional Integral Derivative) control technique, and Ziegler-Nichols engineering setting design, a buck-boost high power and high efficiency driving system based on PID correction network is constructed. The optimized control system greatly improves the response speed, dynamic performance and robustness of the system, and eliminates the steady state error, with strong adaptability to changes in the external environment.

Keywords: Semiconductor lighting; Buck-Boost; PID correction; Engineering setting

1. Introduction

Buck-Boost converter is also known as bucking and boosting converter, as shown in figure 1. It consists of switch tube Q, inductance L, diode D and output capacitance C. The basic idea is to connect a Boost converter behind Buck converter[1-2].so in the application, the single Boost or Buck disadvantages can be overcome, and the “drive dead corner” problem during the low input supply voltage by Buck driver can be also solved, which is widely used in LED drive control system[3-6]. In this paper, according to the working characteristics of Buck-Boost converter, a small signal model of the whole system is established under the voltage mode, and PID control technology and engineering setting method are used to carry out calibration and optimization of the whole closed loop system, then a new type of high power LED drive system is created.

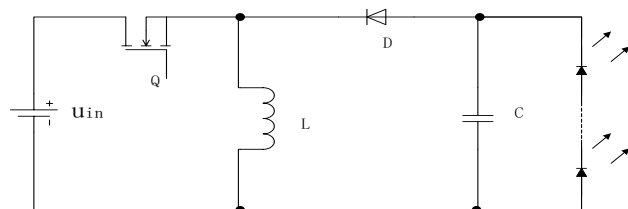


Figure 1: Buck-Boost high power LED driver

2. Voltage mode analysis of Buck-Boost control circuit

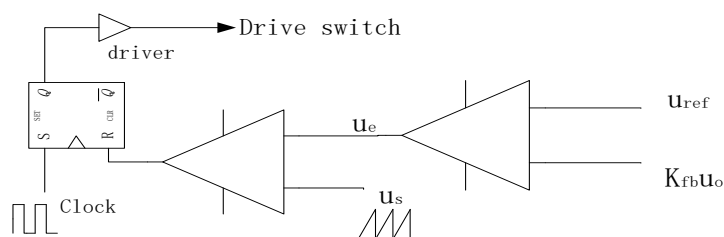


Figure 2: Schematic diagram of voltage mode control

The voltage mode control system is shown in figure 2, after comparative amplification on master

output voltage feedback signal $K_{fb}u_o$ and reference voltage signal u_{ref} , the error voltage signal u_e is gained, it is then added to the inverting terminal of the pulse width modulation comparator, voltage signal u_s is input into its positive end, and the comparator output signal is connected to the reset end of RS trigger, the clock signal Clock is connected with the flip end of the trigger, and the RS trigger end signal will generate switch drive signal after passing driver. At the beginning of each cycle, the clock signal Clock will enable setting of the RS trigger, then switch on, when the output voltage feedback signal $K_{fb}u_o$ increases, if error voltage signal $u_e < u_s$, the comparator will generate high level output to make RS trigger reset, then switch off, waiting until the arrival of a periodic clock signal. As its "control output" system provides a zero and two resonant poles, from the system model analysis, it can be known that the voltage mode control Buck-Boost type LED converter has the following disadvantages [7-8]: (1) there is no voltage feed-forward mechanism for the prediction of the input voltage disturbance, and the response to the input voltage is slower, the control system needs to greatly improve the loop gains [9-10]. (2) The two resonant poles are not compensated and the dynamic response performance is poor.

3. System optimization design of Buck-Boost driver

3.1 PID control setting design

PID control system structure diagram is shown in figure 3. $G_c(s)$ is the transfer function of controller, $G_0(s)$ is the system solid transfer function.

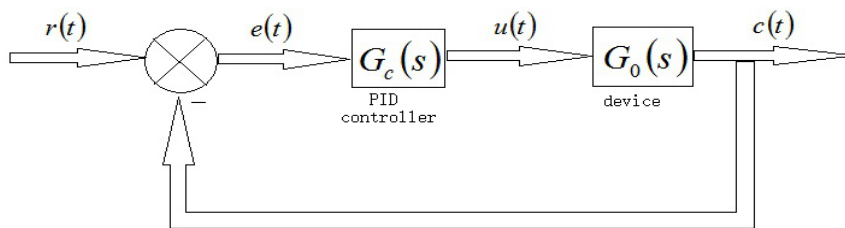


Figure 3: Control system structure with PID controller

PID control is to form a control law after mathematical operation on deviation signal $e(t)$. That is, the controller output:

$$u(t) = K_p \left[e(t) + \frac{1}{T_i} \int_0^t e(t) dt + T_d \frac{d}{dt} e(t) \right] \quad (1)$$

In the formula, K_p is scale factor, $K_p e(t)$ is proportional control item;

$\frac{1}{T_i} \int_0^t e(t) dt$ is Integral control item, T_i is called as integral time constant;

T_d is differential time constant, $T_d \frac{d}{dt} e(t)$ is differential control item.

Sometimes the input and output relations of the PID controller are represented as:

$$u(t) = K_p e(t) + K_i \int_0^t e(t) dt + K_d \frac{d}{dt} e(t) \quad (2)$$

Where, K_p is scale factor, K_i is integral coefficient, K_d differential coefficient.

3.2 Implementation of PID correction network and system simulation analysis

The PID correction network is shown in Figure 4, as seen, two output signals of tracking differentiator 1 are transition differential signal r_2 and transition signal r_1 , and two output signals of tracking differentiator 2 are measuring differential signal f_2 and feedback measurement signal f_1 , then error signal, integral signal of error signal and differential signal of error signal are composed by adder-subtractor to be added to nonlinear combiner, finally, the target control is achieved by the output of nonlinear combiner passing filter.

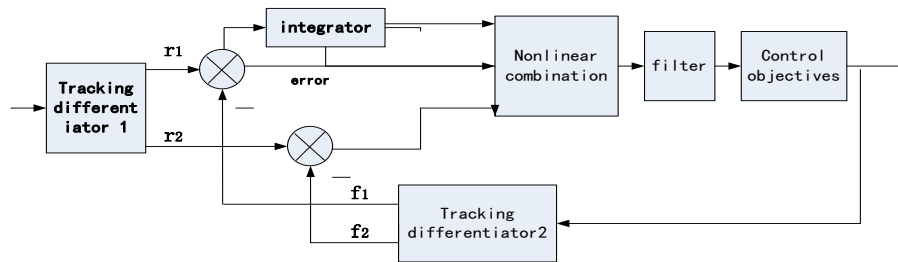


Figure 4: PID correction network

The open loop transfer function of the system is gained by the block diagram of front Buck-Boost voltage mode control system, the Simulink model of the system is shown in figure 5. When disconnecting the system unit feedback line, differential output line and integral output line, the unit step response of open loop system is thus gained, as shown in figure 6.

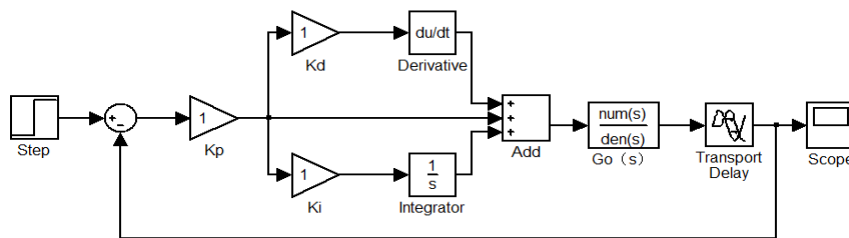


Figure 5: Simulink model of Buck-Boost voltage mode control system

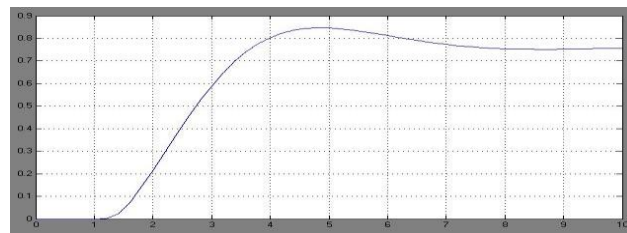


Figure 6: Open loop unit step response of Buck-Boost voltage mode control system

As seen in figure 6, the open-loop step response curve and the S type curve rule can gain the magnification K , time constant T and delay time τ , in order to get more accurate, it can be imported into the work space to write corresponding files to get these three parameters, then, by the closing of wiring and oscilloscope, PI, PI and PID setting are respectively carried out, the unit step responses of each control are shown in the following figure 7-9.

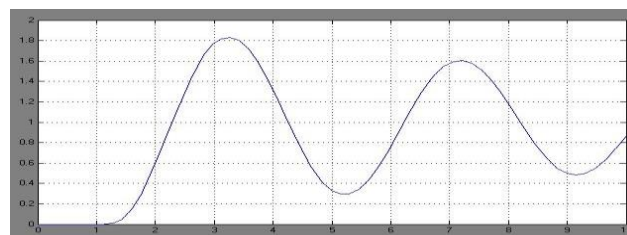


Figure 7: P setting unit step response

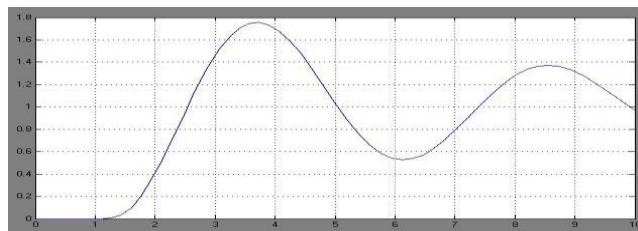


Figure 8: PI setting unit step response

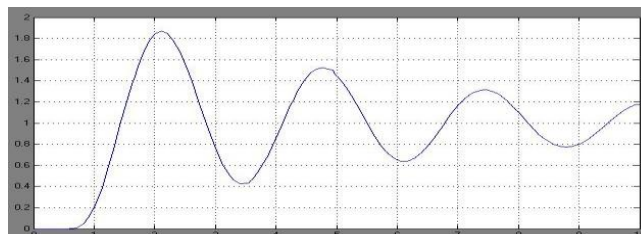


Figure 9: PID setting unit step response

As seen from the dynamic response waveform of above three figures, their waveform response starting point, amplitude and slope are different, while the rapidity of PI and P settings is basically consistent, just because of the difference in the coefficient of proportionality, therefore the system output is different, in terms of overshoot, PI setting is less than P setting, but because of the advantages of these three combined by PID, the response speed is faster and the dynamic performance is better[11-12].

4. Conclusions

In this paper, detailed analysis is conducted on Buck- Boost circuit structure principle performance, such as work patterns under the changes of input, output current, and voltage load; thereupon, the PID control technology is used to carry out system optimization calibration, and by theoretical setting analysis and Ziegler--Nichols engineering setting design, a new buck / boost voltage mode control system based on PID correction network is set up, and then SIMULINK and SIMPOWERSYSTEMS high performance software are used for simulation study, it is found that this control system can greatly improve the response speed, robustness and adaptability of the external environment.

Acknowledgements

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References

- [1] Ma H, Namgoong G, Choi E, et al. Instantaneous power consuming level shifter for improving power conversion efficiency of buck converter [J]. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2018, 66(7): 1207-1211.
- [2] Liu Z, Cong L, Lee H. Design of on-chip gate drivers with power-efficient high-speed level shifting and dynamic timing control for high-voltage synchronous switching power converters[J]. *IEEE Journal of Solid-State Circuits*, 2017, 50(6): 1463-1477.
- [3] Lee S Y, Liao Z X, Lee C H. Energy-harvesting circuits with a high-efficiency rectifier and a low temperature coefficient bandgap voltage reference [J]. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2019, 27(8): 1760-1767.
- [4] Ming X, Fan Z, Xin Y, et al. An Advanced Bootstrap Circuit for High Frequency, High Area-Efficiency and Low EMI Buck Converter [J]. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2019, 66(5): 858-862.
- [5] T. Karaca, M. Auer. A Class-D output bridge with dynamic dead-time, small delay and reduced EMI[C]//, *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, 2017, 1-4
- [6] Wittmann J, Barner A, Rosahl T, et al. An 18 V input 10 MHz buck converter with 125

- psmixed-signal dead time control [J]. IEEE Journal of Solid-State Circuits, 2020, 51(7): 1705- 1715.*
- [7] Zhou Z, Yuan Y, Wang Y, et al. A Predictive Gate Driver Suitable for Half-Bridge Applications [C]// 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD). IEEE, 2019: 131-134.
- [8] Kim S Y, Park Y J, Ali I, et al. Design of a high efficiency DC–DC buck converter with two-step digital PWM and low power self-tracking zero current detector for $I_o T$ applications [J]. IEEE Transactions on Power Electronics, 2017, 33(2): 1428-1439.
- [9] Woo K C, Oh J M, Yang B D. DC–DC Buck Converter Using Analog Coarse-Fine Self-Tracking Zero-Current Detection Scheme [J]. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66(11): 1850-1854.
- [10] Liu D, Hollis S J, Dymond H C P, et al. Design of 370-ps delay floating-voltage level shifters with 30-V/ns power supply slew tolerance[J]. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 63(7): 688-692.
- [11] Lehmann T. Design of fast low-power floating high-voltage level-shifters [J]. Electronics letters, 2017, 50(3): 202-204.
- [12] Liu D, Hollis S J, Stark B H. A new design technique for sub-nanosecond delay and 200 V/ns power supply slew-tolerant floating voltage level shifters for Ga N SMPS [J]. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 66(3): 1280-1290.