Academic Journal of Materials & Chemistry
ISSN 2616-5880 Vol. 4, Issue 7: 69-76, DOI: 10.25236/AJMC.2023.040711

Prospect for Overcoming Sub-threshold Slope Degradation with NC-FETs

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Abstract: *For conventional MOSFETs, with the reduction in the thickness of silicon dioxide, the value of subthreshold swing has reached 60 mV/dec, a minimum constrained by thermodynamics. Hence, further scaling of transistor necessitates novel approaches while maintaining high performance. So far, there are three main parallel paths of overcoming sub-threshold degradation, which are enhancing gate control, using the band-to-band tunneling (BTBT) mechanism and change the capacitance of oxide layer, the corresponding solutions are FinFET/gateall-around FET(GAAFET), tunnel FET(TFET) and negative capacitance field-effect transistor (NC-FET), respectively. This paper mainly explores the feasibility of utilization of NC-FETs as a promising solution with the Ferroelectric-Dielectric materials, thereby evaluating the prospect of NC-FETs as a potential candidate to continue reducing sub-threshold slope degradation. Several critical issues of NC-FETs that are not favorable to application due to their intrinsic features, such as hysteresis, are analyzed, including the latest research efforts aimed at tackling those problems.*

Keywords: *NCFET, Ferroelectrics, Hysteresis*

1. Introduction

With the scaling of transistors, the static power dissipation has become a severe issue, as a result of the off-state current, I_{off} flowing between the drain to source in MOSFETs (Figure 1). The sub-threshold current that exists when $V_{GS} < V_T$, mainly contributes to that leakage. Ideally, the Drain-to-Source Current (I_{ds}) falls to 0 when V_{GS} decreases from V_T to 0. However, it degrades exponentially while eventually staying above 0, resulting in I_{off}, which involves a dominant term $\cdot 10^{-V_T/S}$. Here S refers to the Sub-threshold Swing——the inverse of the sub-threshold slope representing the rate that FETs switch from cut-off region to linear region when $V_T < V_{GS}$. I_{off} exists if there is a source voltage. The power consumption caused by I_{off} is static power dissipation. Although the Power Gating techniques, namely, turning off the voltage source when FETs are at cut-off region can avoid this issue, it requires considerable complexity and careful timing analysis [1]. As a result, minimizing I_{off} is a once-and-for-all way to cut down static power dissipation. The threshold voltage is incompressible, otherwise it will provide an exponential gain to I_{off} leakage, which conflicts with the pursuit of reducing static power dissipation. Along with the increase of V_{GS}, at the time $I_{ds} > I_{on}$, the transistor is on. Since the time for charging gate capacitance is constant, greater sub-threshold slope results in less time consumption for I_{ds} reaching I_{on} to attain the "switch-on" level to obtain higher operating frequency, ultimately enhancing overall performance. Hence, overcoming sub-threshold slope degradation (i.e. reducing Sub-threshold Swing S) is desirable for both power dissipation problem and operating frequency problem.

As the channel length becomes shorter to sustain scaling, the distance between drain and sources shortens. The band of channel is pulled down, lowering down the potential barrier height, which allows more electrons to flow into the channel. Then the gate is harder to control the channel. The sufficient V_{GS} that degrades barrier height to allow channel current defines the threshold voltage V_T above. To precisely describe this phenomenon of short channel effect (SCE), many models were raised to mathematically describe the behavior of I_{ds} along the path of scaling, such as charging sharing models, empirical expressions, polynomial potential models and analytic solutions to 2-D Poisson's equation [2]. Three categories of solutions of FETs were developed to overcome the impact caused by SCE. In this overview, only NCFET will be concretely explained.

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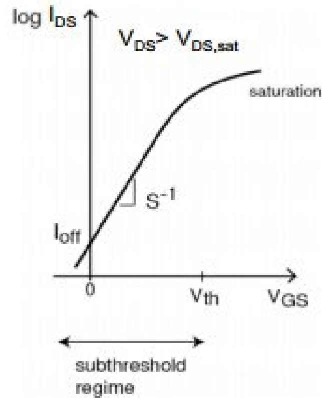

Figure 1: Logarithm relation between drain to source current and gate to source voltage [3]

2. Key Determinants of SS and Corresponding Solutions

To effectively decrease *SS*, there are three main methods.

2.1 FinFET

First, it can be decreased by enhancing gate control. The desire of Gate controllability over the channel leads the semiconductor technology move towards the multi-gate MOSFETs. The FinFET is a unique structure for FETs to realize this objective. Its additional gates improve the drain potential screening from the channel [4–6]. Fully depleted double gate SOI structure was firstly raised by Hisamato et. al. in 1989 [7]. Subsequent research has demonstrated that FinFETs exhibit a number of excellent qualities such as maintaining a steep subthreshold slope, better performance with bias voltage scaling and good matching due to low doping concentration in the channel [8], which allow them to be put to use in the production and utilization of COMS technology. However, compared with planar MOSFET, FinFET has some insurmountable problems, including high access resistance caused by extremely thin body, implementation of strain boosters and difficulties related to the non-planar structure [8]. Though the well-developed planar CMOS manufacturing is also feasible for the fabrication process of FinFET, much stricter process control is required during the stages of patterning the fin and the gate. The thin fin of the transistor and the formation of 3D structures result in high access resistance and undesired parasitic resistance, imposing a detrimental effect on high-frequency circuit.

2.2 TFET

Then, *SS* can be controlled by replacing heating electrons with band-to-band mechanism. In this way, the physical limitation of MOSFET can be overshot. Quantum mechanical tunneling is a physical effect that a number of electrons in low energy band can break potential barrier and appear in high energy band. TFET obeys band-to-band tunneling mechanism in PN junction with the quantum-mechanical generation of carriers [9], meaning that the movement of electrons is determined by tunneling through the barrier, which is different from mechanism of ordinary FET that is diffusing over the barrier potential. So far, many structures of TFET has been developed, such as feedback TFET, p-n-i-n TFET, dopingless PNPN TFET, hetero-structure TFET, etc. TFET has the potential to go beyond the limit of < 60mV/dec *SS*, but it yet meets several problems. One of the largest concerns is that the drive current of TFET may be not big enough due to the influence of its high tunneling resistance. High off-state leakage is another problem due to the ambipolar behavior of TFET. Tejas Krishnamohan et. al. [10] said that lateral hetero-structure TFET is the most promising structure to solve the mentioned problems, but there are still some researches going on in this area to mature TFET.

2.3 NCFET

Last, for NCFET, the *SS* is determined by two terms in addition to the ambient temperature as the following mathematical expression (Figure 2):

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$$SS(mV/dec) = \frac{\partial V_G}{\partial \, log_{10} I_D} = \frac{\partial V_G}{\partial \psi_s} \frac{\partial \psi_s}{\partial \, log_{10} I_L} = \eta \cdot 60 \; mV \cdot \frac{T}{300K}$$

$$\eta \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_{ins}}{C_s}$$

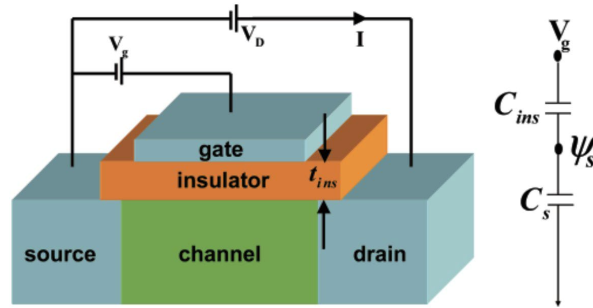

Figure 2: A nice capacitance divider [11]

The theoretical minimum value of SS attained by the conventional MOSFETs at room temperature is 60 mV/dec, which usually refers to "Boltzmann's Tyranny" for the thermodynamic constraint. Some proposals to overcome SS degradation make compromises with the existence of that physical constraint, thus focus on the second term $\frac{\partial \psi_s}{\partial \log_{10} I_L}$. To reach this limit, C_{ins}, i.e. the capacitance of insulator (usually silicon dioxide) should be as low as zero, which is impossible for normal MOSFET, however, suppose C_{ins} becomes negative, then η will be smaller than 1, thereby lowering the value of SS down below 60 mV/dec. With the help of ferroelectric material embedded in gate, in dynamic process, this consumption can be realized.

3. Physical Mechanism of Ferroelectric that Induces Negative Capacitance

The phenomenon of negative capacitance was often regarded as "anomalous" or "abnormal" at the time when limited reports and research were available. Instances of measured negative capacitance were incorrectly ascribed to instrumental errors [12]. However, as time progressed, a deeper understanding of the underlying mechanism and the potential implications of negative capacitance gradually emerged, though still remains a topic of controversy, which mainly revolves around two emphases. One is the prevailing theory of stabilized S-shaped polarization-electric field ($P-E$) curve, the other is the delay of ferroelectrics (FE) polarization switching [13]. Nevertheless, both theories are rooted in the key properties of ferroelectrics, which will become the priority of this discussion.

3.1 Stabilized S-shaped Polarization-Electric Field (P−E) Curve

The general behavior of ferroelectrics can be explained by Landau-Khalatnikov(LK) theory stating that

$$\rho \frac{d\vec{P}}{dt} + \nabla_{\vec{P}} G = 0$$

Here ρ, P, and t respectively denotes resistivity, polarization, and time. And G is the Gibb's free energy, the sum of Anisotropic energy (i.e. "directionally dependent") and the energy due to external field E_{ext}, which is defined by Landau-Devonshire theory as

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - \vec{E}ext.\vec{P} \; in \, which \, \alpha = \alpha_0(T - T_0), \alpha_0 > 0$$

T_0 denotes the Curie temperature. And thereby the external electric field E_{ext} is obtained by combining two equations above.

$$Eext = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt}$$

If ferroelectric operates in steady-state polarization, then $\rho \frac{dP}{dt} = \frac{\partial G}{\partial P} = 0$, leading to time-independent ($P-E$) relation between polarization and electric field. [13,14] Moreover, we obtain the ($G-P$) relation

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that explains the behavior of paraelectric and ferroelectrics mathematically. While removing the applied field E_{ext}, the equation $2\alpha P + 4\beta P^3 + 6\gamma P^5 = 0$ is solved respect to each case. For paraelectric with $(T > T0, i.e. a > 0)$, there is a unique solution that $P = 0$. Hence, for the conventional paraelectric materials, there is no dielectric polarization while removing the electric field. By contrast, α is negative (i.e. $T < T_0$) when the temperature decreases beyond a specific threshold (Curie Temperature). There are three real roots exist for P, among which the two non-zero real roots represent each possible state of polarization:

$$P = 0,$$

$$P_r = \pm\sqrt{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$$

That result corresponds to the observation of the unit cell of ferroelectric crystalline materials, which exhibits non-centrosymmetricity, arising spontaneous permanent polarization with two states without being induced by external electric field. However, the direction of such polarization is reversible. The state can be switched by applying external electric field stronger than intrinsic coercive field of the ferroelectrics.

Moreover, according to the established definition of capacitance for general dielectric materials, denoted as

$$C = (\frac{\partial^2 G}{\partial Q^2})$$

wherein G represents energy density, and Q indicates charge density, the segment displaying

Negative curvature on the G–P (energy density - polarization) plot corresponds to the range in which capacitance assumes a negative value.

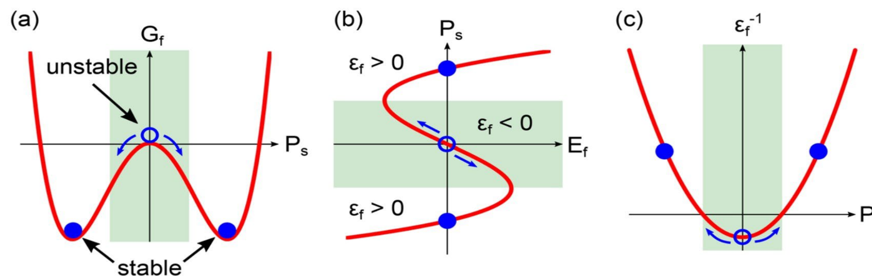

Figure 3: (a) The free energy polarization distribution when Ef = 0. (b) Polarization-electric field dependence. (c) Inverse of ϵF as a function of polarization. It is thermodynamically unstable in the negative permittivity region. [15]

It can be observed from figure 3(a) that the region of negative permittivity is unstable. Within this region, the free energy attains its peak, indicating that the state of negative capacitance is transient. Two solutions have been raised towards this issue. Firstly, alternating the ferroelectric polarization between two distinct stable states through the application of mutable electric field is considered. Secondly, the ferroelectric material can be integrated into a larger structure, thereby minimizing the total free energy of the system and enabling the sustenance of the negative capacitance state. [15].

It still requires effort for researchers to put NCFET into practical implementation. Most of ferroelectric materials realize the function of switch on and off by irreversible domain nucleation and growth mechanisms. Their behaviors lead to the manifestation of polarization hysteresis, preventing FETs made of such negative capacitance materials from operating at high frequencies with low voltage. Hence, a voltage-time trade-off [14] existing in the transition of NCFET from one stable state to another. When this transformation occurs rapidly, it demands a higher voltage input, resulting in increased power consumption and heat generation. Consequently, the application of transient NC transitions becomes impractical for high-speed digital electronic operations. Stabilize the intrinsic NC state, if feasible, could effectively address the issue of hysteresis, enhancing the practical potential of NCFETs in high-performance circuit.

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3.2 Delay of FE polarization switching

In addition to utilizing a series combination of ferroelectrics and dielectrics within the gate stack of a NCFET to achieve a stable negative capacitance (NC) state, recent studies have shown that the NC effect can also manifest in an independent ferroelectric (FE) capacitor. This discovery challenges previous argument that this phenomenon was not measurable due to the thermodynamic stability constraints outlined in established theories, highlighting that the physics origin of the NC effect lies in the dynamic process of domain switching within the ferroelectric material. Notably, the NC phenomenon is strongly associated with voltage FE voltage V_{FE} and sweeping rate. [13]

This proposal needs modification of mathematical expression of Subthreshold swing, from which the internal voltage amplification A_V is obtained as another determinant that reduce *SS* down below 60 $mV \cdot dec^{-1}$:

$$SS = \frac{\partial V_G}{\partial log_{10} I_D} = \frac{\partial V_G}{\partial V_{int}} \frac{\partial V_{int}}{\partial \varphi_s} \frac{\partial \varphi_s}{\partial log_{10} I_D}$$

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{1}{C_P} \frac{dP}{dV_G}$$

And the polarization of FE is characterized by Kolmogorov-Avrami-Ishibashi equation as a function of V_{FE} and *T*.

$$\frac{dP}{dV_G} = \frac{\partial P}{\partial t} \frac{dt}{dV_G} + \frac{\partial P}{\partial V_{FE}} \frac{V_{FE}}{dV_G}$$

Substituting $\frac{dP}{dV_G}$ above into the expression of A_V, we get:

$$A_V = \frac{1}{C_P} \left(\frac{\partial P}{\partial t} \frac{dt}{dV_G} + \frac{\partial P}{\partial V_{FE}}\right) \Big/ dV_G$$

$$A_V = \left(\frac{\partial P}{\partial t} \frac{dt}{dV_G} + \frac{\partial P}{\partial V_{FE}}\right) \Big/ \left(\frac{\partial P}{\partial V_{FE}} + C_P\right)$$

In order to accomplish *SS* reduction, A_V has to be greater than 1. Therefore, the ensuing inequality must be satisfied:

$$\frac{\partial P}{\partial t} > \frac{C_P \cdot \partial V_G}{\partial t}$$

This relationship constitutes the basis of “dynamic polarization matching”, in which the time-induced increment of polarization $\frac{\partial P}{\partial t}$ directly determines the steepness of *SS*. The sweeping rate denoted as $\frac{\partial V_G}{\partial t}$ must be constrained within certain range, otherwise it will result in subthreshold slope degradation. [13]

4. Issues Brought by Hysteresis of Transient NCFETs and Possible Solutions

4.1 The mechanism of hysteresis

Hysteresis in ferroelectric materials often refers to polarization hysteresis. The crystal structure of ferroelectric material determines its ferroelectricity that it has spontaneous polarization. The direction of electric dipole moment can be changed by applied electric field. The electric dipole moment in ferroelectric materials needs to be redirecting to reach a transient NC. Since this is a process of turning the direction of whole lattice, compared to simply accelerate electrons to open the channel for MOSFET, it consumes much more time and energy. The time delay that the rotation cost is indispensable, so it will be a problem for high-frequency circuit for the NCFET to keep in NC region.

Figure 4 illustrates the trend when sweeping V_G with different rates at different starting voltage V_{sta}. It can be observed that the voltage at the ferroelectric layer V_{FE} in NCFET is strongly related to the sweeping rate and range of V_G. Figure 5 is a comparison between transient NCFET with normal MOSFET. The hysteresis of NCFET always exists theoretically and shows counterclockwise behavior. Figure 6 shows that both slower V_G sweeping rate and the faster FE switching response can massively reduce the hysteresis of transient NCFET but cannot be totally avoided. Based on above analysis, smaller hysteresis and SS can be reached by smaller V_{FE} and quicker polarization changing frequency. However, intrinsic

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optimization conflict exists between these two factors. So, more effort is needed to overcome hysteresis in transient NCFET.

4.2 The Latest Efforts for Obtaining Hysteresis-Free NCFETs

Hysteresis might be totally avoided by stabilized negative capacitance. In [14], a method was mentioned that ferroelectric NC can be stabilized by adding a positive capacitance in series. However, this thought has been

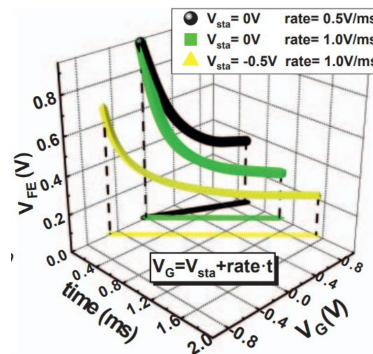

Figure 4: VFE vs t in NCFET at various VG with different rates and Vsta. [13]

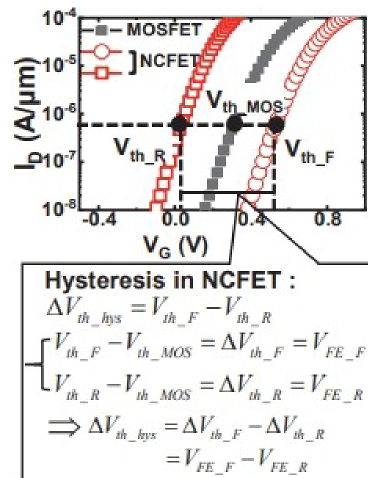

Figure 5: The Vth relationship between the hysteresis of NCFET and the MOSFET [13]

Proved impossible because of the effects of leakage currents and domain formation. But other effort has been made. The free energy of the dielectric can be written as

$$G_d = \frac{D^2}{2\varepsilon_0\varepsilon_d} - DE_d$$

Here, D is the displacement field. And under the consumption that $D = P_s$, the total free energy can be written as

$$G_t = G_f t_f + G_d t_d = \left(\alpha t_f + \frac{t_d}{2\varepsilon_0\varepsilon_d}\right) P_S^2 + t_f \beta P_S^4 - \mathrm{V} P_S$$

Here t_f is the ferroelectric thickness and t_d is the dielectric thickness. When NC is stable, the condition

$$t_f \le t_{f,crit} = -\frac{t_d}{2\alpha\varepsilon_0\varepsilon_d}$$

In figure 7(b), when V = 0, it is still a positive capacitance, When V is increased larger than V_c in figure 7(d), P_s switches to positive, causing a severe decrease in the field in the ferroelectric. So, it becomes a transient NC. And in figure 7(g), $t_f \le t_{f,crit}$, it can be observed from figure 7(h)-(l), the whole process is stable since there is no negative curvature of G_t. As a result, this working route does not include hysteresis. These analysis means that by choosing proper ferroelectric and dielectric thickness, hysteresis can be avoided. To reach this condition and satisfy the requirement of scaling, proper material should be

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carefully choosing to construct NCFET.

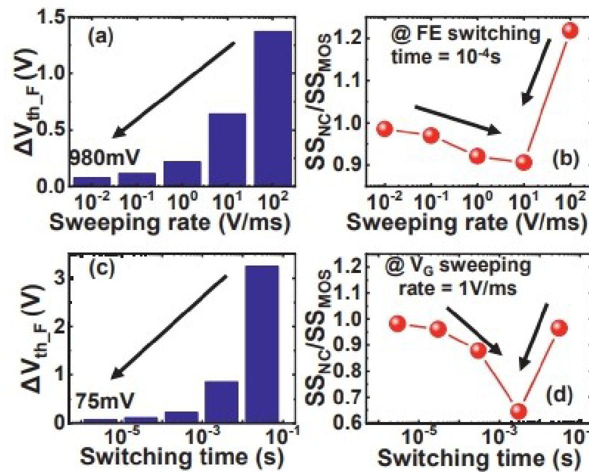

Figure 6: Different (a) (b) sweeping rate of VG and (c) (d) switching time of FE [13]

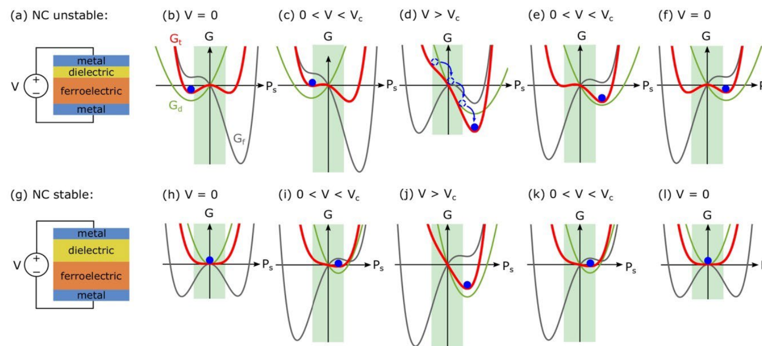

Figure 7: Stabilization of NC with applied voltage V.(a)NC is unstable if the dielectric layer is too thin (g)The NC state is stabilized by the energy of the dielectric at V = 0 [15]

5. Conclusion

In this review, we first present the fundamental determinant of subthreshold swing and subsequently provide an overview of three main current proposals as potential candidates to overcome subthreshold slope degradation, among which the Negative Capacitance FET is the emphasis of our discussion. Our following analysis derived from the underlying physics mechanisms inherent to ferroelectric materials that induces negative capacitance phenomenon, which still remains a topic of controversy. And we exhibit the current focus for explanation respectively, from which the hysteresis manifest as a pervasive phenomenon while approaching the stable NC state, poses a significant barrier that impedes the implementation of NCFETs. Recent studies have revealed that this issue can be effectively tackled through the manipulation of the thickness of both the ferroelectric and oxide layers. This adjustment leads to the negative slope within the free energy function, ultimately eliminating the impact of hysteresis. In general, the focus of future research will concentrate on the selection of suitable materials that can satisfy such requirement.

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