International Journal of Frontiers in Engineering Technology
ISSN 2706-655X Vol.6, Issue 6: 59-65, DOI: 10.25236/IJFET.2024.060609

Analysis of heat-stress coupling field and optimisation strategy for IGBT power converters

Fei Wu[1,*], **Zikang He**[2]

[1]*School of Electrical Engineering, Xinjiang University, Urumqi, 830049, China*
[2]*School of Electrical Engineering, Tongda College of Nanjing University of Posts and Telecommunications, Yangzhou, 225100, China*
[*]*Corresponding author: 13853002795@163.com*

Abstract: *With the continuous development of new power systems, the insulated gate bipolar transistor (IGBT) has become the core component of power converters. Its failure rate has a critical impact on the safety and stability of the overall operation of the circuit. Frequent failures will not only result in equipment downtime, but may also lead to more serious system failures. Therefore, in this paper, the finite element analysis software COMSOL is used to construct the thermal-stress coupling field model of IGBT, and the stress caused by the thermal field is analysed over the lifetime of the IGBT device. The results show that the increase of heat flux promotes the heat flow, which reduces the surface temperature of the IGBT chip, and then relieves the stress at the root of the bonding line and the edge of the solder layer. The closer the thermal expansion coefficient between the contacting materials, the more the expansion rate tends to be the same as the temperature rises, and finally the stress reduction effect is achieved. The experimental results provide a theoretical and data basis for reducing the stress at the root of the bonding wire and at the edge of the solder layer, thereby extending the life of the IGBT.*

Keywords: *IGBT, Thermal-Stress Coupling Field, Thermal Expansion Coefficient, Heat Flux*

1. Introduction

In the late 1980s, a new type of power semiconductor device, the insulated-gate bipolar transistor (IGBT), was successfully developed. In comparison to MOSFET, IGBT exhibits a number of advantages, including rapid switching speed, low saturation voltage drop, lower power consumption and enhanced thermal stability. Additionally, it possesses the characteristics of a simple driving unit, lower conduction voltage, higher input impedance and the capacity to withstand high voltages and large currents. Consequently, IGBT power modules are also extensively employed in the majority of power conversion devices, occupying a pivotal role in numerous application scenarios, including electric vehicles, smart grids, high-speed rail, aerospace and aviation.

As the central device, the stability and failure rate of IGBT directly affect the normal operation of the power system. Given that IGBT modules typically operate in challenging environments with high voltage and high current, faults and damage issues frequently arise in applications, significantly limiting their deployment and advancement. Previous studies have extensively explored IGBT module fault analysis and diagnosis. Luo et al. [1] employed the COMSOL software to develop and examine the multi-physical field coupling theory of IGBT, encompassing the mutual coupling of electric and thermal fields, as well as the influence of thermal fields on mechanical fields. The principle of thermal deformation of the IGBT module has been elucidated, and it has been determined that the dynamic and static thermal deformation exhibit an initial increase followed by a stabilisation phase. Xue et al. [2] focused on the general and specific faults resulting from IGBT overheating, outlined the conventional protection method, and developed an integrated system and experimental platform for monitoring and analysing IGBT overheating faults on the basis of theory. Sun et al. [3] conducted a numerical study on the thermal effect of IGBT under single pulse and periodic electromagnetic pulses, and analysed the temperature field of IGBT under different ageing states of the solder layer. To date, there has been no comprehensive investigation into the optimisation and protection of IGBT through the utilisation of IGBT thermal-force field coupling fields.

In light of the aforementioned considerations, the research object selected in this paper is the welded IGBT module. Based on the structure and working principle of IGBT, a three-dimensional thermal-force field coupling model of IGBT is constructed using the finite element analysis software COMSOL. Under the working conditions, the material properties are studied with a view to optimising the distribution of temperature and stress fields and alleviating the ageing problem caused by the stress of the bonding bond and solder layer[4-6].

2. Experimental platform and method

2.1 The structure of IGBT

Prior to undertaking further optimisation of the IGBT, it is essential to gain a comprehensive understanding of its fundamental structure and operational principles. The IGBT module under investigation is primarily constituted by two IGBT chips and two freewheeling diode (FWD) chips. The IGBT power module is comprised of an IGBT chip and a freewheeling diode (FWD) chip, as illustrated in Figure 1. From the top to the bottom, the components are the IGBT chip, the diode chip, the upper solder layer, the direct bonded copper (DBC) upper copper layer, the DBC ceramic layer, the DBC lower copper layer, the lower solder layer and the copper substrate.

The IGBT and diode chips in the module are connected to the circuit on the DBC copper layer by welding, while the power circuit is connected by bonding wire. To enhance the load capacity of the IGBT module and diminish the impedance of the electrical connection, it is common practice to utilise multiple parallel aluminium wires. The lower copper layer of DBC is welded with the lower copper substrate to form a mechanical support structure for the module. This structure provides electrical insulation and effectively transfers heat to the copper substrate.

The upper solder layer connects the chip to the upper copper layer of the DBC, and the lower solder layer connects the lower copper layer to the copper substrate, thereby forming a stable internal structure while conducting heat between different structures. The package is filled with silicone in order to achieve insulation, impact resistance and good thermal conductivity.

Finally, the simulation model is obtained in the finite element analysis software COMSOL, as shown in Figure 2.

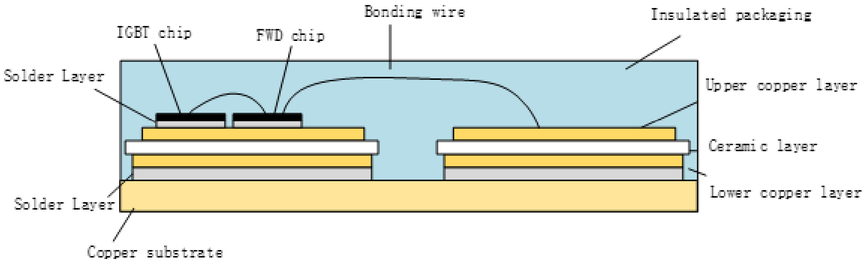


Figure 1: IGBT structure

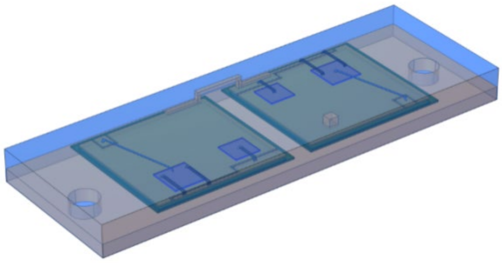


Figure 2: IGBT structure in COMSOL

2.2 The establishment of thermal field boundary constraints

Figure 3 illustrates the schematic diagram of the IGBT module thermal field boundary condition setting. In the context of the heat transfer analysis, it is reasonable to assume that the bottom of the copper substrate is in close contact with the heat dissipation silicone grease during the actual operation of the IGBT module. Consequently, the bottom of the copper substrate can be considered as the boundary of the convective heat flux, with a heat transfer coefficient of 300 W/(m²·K). The initial temperature was set to 298.15 K. As the IGBT chip and the FWD chip will generate power loss during operation (only the main heat source IGBT chip is considered), the IGBT chip is designated as the heat source boundary, with a heat consumption rate of 30 W.

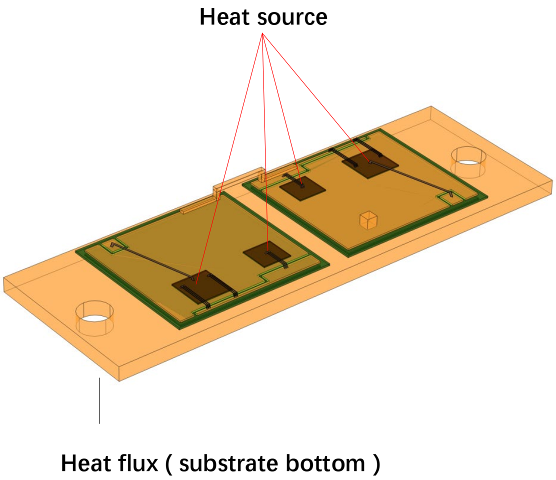


Figure 3: Thermal field boundary constraints

2.3 The establishment of boundary constraint conditions of stress field

Figure 4 illustrates the boundary constraint condition of the stress field of the IGBT module. The bottom of the copper substrate and the screw hole are designated as fixed constraints, whereas the remaining components are regarded as free boundaries. The initial displacement field is set to zero, and the thermal expansion boundary encompasses the entire region. Concurrently, thermal expansion is incorporated into the linear elastic material[7-9].

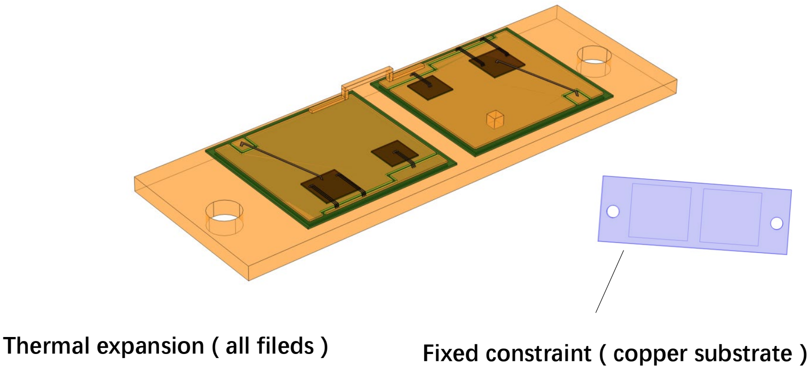
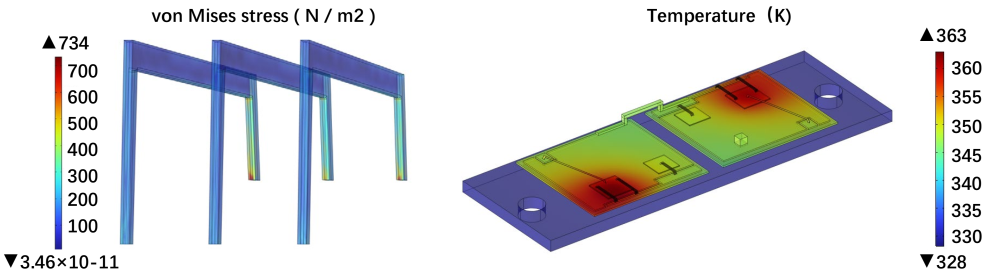


Figure 4: Boundary constraints of stress field

3. Results and discussion

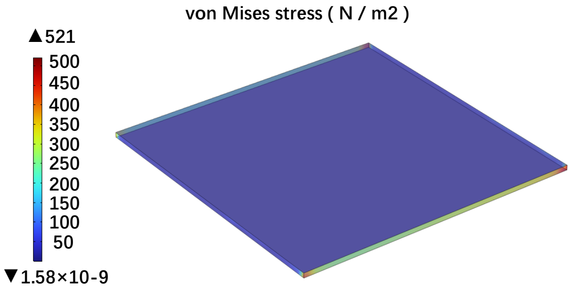
3.1 Multi-physical field analysis of IGBT

The thermal-mechanical coupling multi-physical field of the IGBT, calculated based on COMSOL, is illustrated in Figure 5. The results demonstrate that the thermal field is predominantly concentrated in the IGBT chip position, with a maximum temperature of 363 K. A decreasing trend is observed from the centre of the IGBT chip to the edge position. It is noteworthy that the thermal conductivity of the DBC ceramic layer is significantly higher than that of the solder layer, resulting in a markedly lower surface temperature of the DBC in comparison to the solder layer. With regard to the force field, it can be observed that the edge of the chip is subjected to considerable mechanical stress as a consequence of the thermal expansion coefficient. Upon extracting the edge position of the chip separately, it becomes evident that the stress is primarily concentrated on the edge of the solder layer and the root of the bonding line.



The Von stress of the bonding wire under the heat transfer coefficient of 300 W / (m²·K)

The IGBT chip shell temperature under the heat transfer coefficient of 300 W / (m²·K)



The stress of solder layer under the heat transfer coefficient of 300 W / (m²·K)

Figure 5: Unoptimized thermal-mechanical coupling field distribution

In the unoptimised IGBT thermal-mechanical coupling field distribution model, through data and graphic analysis, the following key points can be obtained:

1) Heat distribution:

The upper image shows the surface temperature distribution of the welded IGBT module, and the maximum temperature reaches 363 K. It is evident that there is a considerable accumulation of heat near the IGBT chip, which then decreases in concentration from the centre position of the IGBT chip to the edge position.

2) Stress distribution:

Figure 5 illustrates the distribution of stress in the chip solder layer, with a maximum value of 521 N/m². This suggests that when subjected to thermal loads, the chip shell experiences considerable mechanical stress, which could potentially result in material fatigue or failure. The maximum stress observed in the bonding wire is 734 N/m². This value suggests that the bonding wire may be susceptible to fracture under operational conditions.

The data and graphics illustrate that there is a notable accumulation of heat and concentration of stress within the thermal-force field distribution under the unoptimised state, which may have a detrimental impact on the long-term reliability of the equipment. It is therefore necessary to optimise the thermal management strategy in order to reduce the stress and improve the uniformity of heat distribution[10-12].

3.2 Analysis of experimental results

In the simulation experiment, two principal material properties were selected for investigation: heat flux and coefficient of thermal expansion (CTE). The experimental data demonstrate that the heat flux exerts a considerable influence on the research objectives.

3.2.1 Study on heat flux

In the heat flow study, the bottom surface of the copper substrate is set as the convective heat flow boundary, with a heat transfer coefficient of 300 W/(m²·K) as the control group. Four experimental groups are selected, with heat transfer coefficients decreasing by 50 W/(m²·K) to the left and right of the control group, in order to observe changes in the shell temperature of the IGBT chip, as well as stress variations in the bond wire and solder layer. The simulation results for the maximum shell temperature, maximum Von stress in the bond wire and maximum Von stress in the solder layer for the control group are shown in Figure 6. The simulation results for the experimental groups are plotted on a dot line plot as shown in Figure 7.

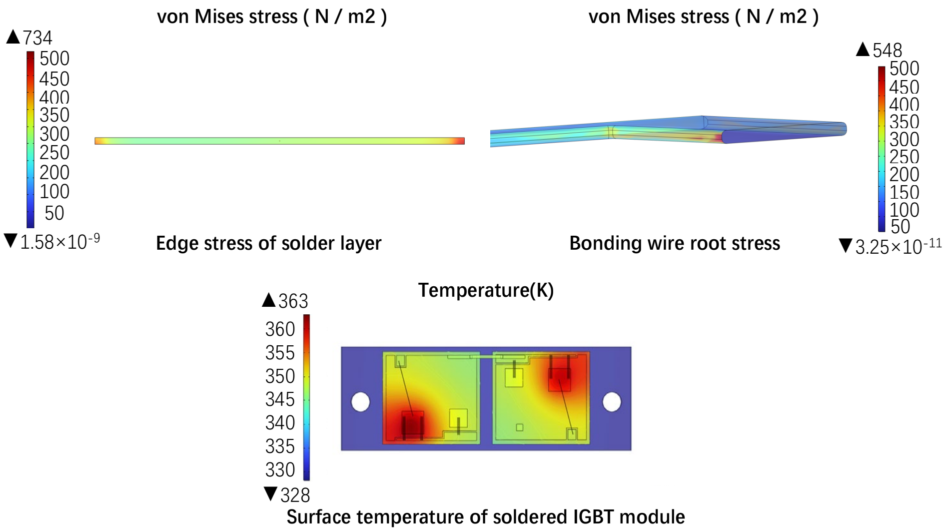


Figure 6: The heat transfer coefficient of the control group was 300 W / (m² · K)

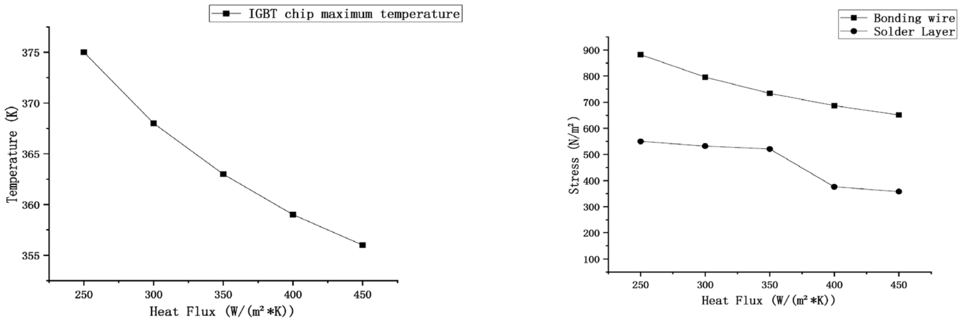


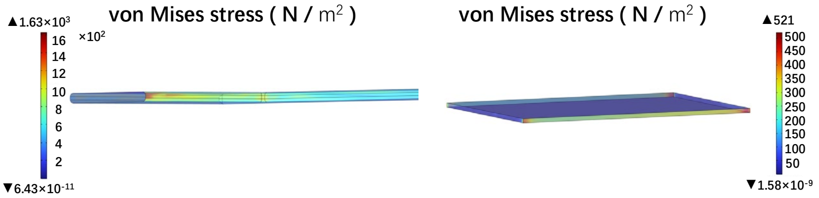
Figure 7: Comparison of experimental group data

The results illustrate the temperature distribution and stress experienced by the IGBT module under operational conditions. To illustrate, the maximum temperature of the IGBT chip depicted in Figure 6 reaches 363 K, while the solder layer and the bonding wire in close proximity to it attain the higher stress values of 521 N/m² and 548 N/m², respectively, at the root and edge.

The results demonstrate that with an increase in heat flux, although stress remains concentrated at the edge of the chip (the edge of the solder layer and the root of the bonding line), the overall trend is still a decrease. A change in heat flux from 200 W/(m²·K) to 400 W/(m²·K) results in a 5.6% change in stress at the edge of the solder layer and a 35% change in stress at the bonding line junction. This is due to the fact that a change in heat flux facilitates the effective flow of heat, thereby preventing the accumulation of heat near the source. Furthermore, the stress levels in the vicinity of the solder layer and the bonding wire are also diminished. It can be inferred that there is a notable negative correlation between the heat flux and the surface temperature of the IGBT chip. The alteration in heat flux exerts a considerable influence on the alleviation of solder layer and edge bonding line stress by reducing temperature.

3.2.2 Study on heat CTE

In the study of CTE, the bonding wire and the solder layer at the bottom of the chip are employed as conditional constraints, with the CTE of the material itself designated as the control group. The array values are selected between the CTE of the IGBT chip and the copper substrate connected by the bonding wire (the research on the solder layer is conducted in a similar manner) in order to observe the stress changes of the bonding wire and the solder layer. The maximum Von stress of the bond line and the maximum Von stress of the solder layer in the control group were simulated, as illustrated in Figure 8. The experimental group simulation experiment diagram was recorded and is presented in Figure 9.



The maximum VON stress of bonding wire and solder layer when IGBT chip is normal model material

Figure 8: The VON stress of bonding wire and solder layer

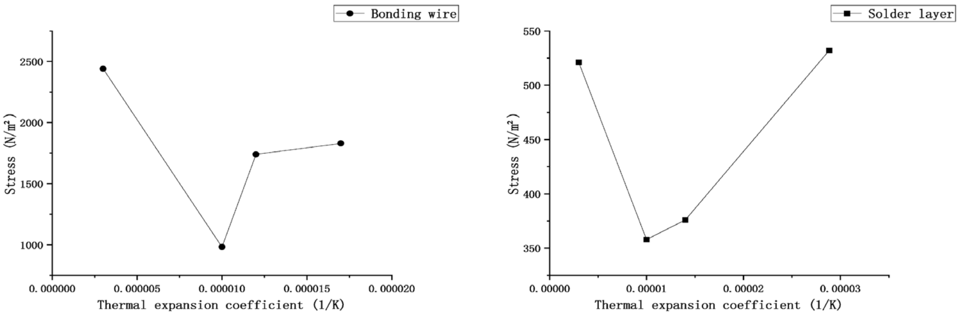


Figure 9: Comparison of experimental group data

The results demonstrate that the stress experienced by the IGBT module under different thermal expansion coefficients, including the solder layer and the bonding wire (as illustrated in Figure 8), reached a higher Von stress value of 521 N/m² and 1630 N/m² at the root and edge, respectively.

In this study, the thermal expansion coefficient of the bonding wire and the solder layer was varied between the coefficients of copper and silicon, and the results are presented in Figure 9. As the thermal expansion coefficient increased, the von stress initially decreased and then increased. A value of the thermal expansion coefficient between the sandwich materials can be identified as a means of minimising the Von stress. It can therefore be concluded that when the thermal expansion coefficients of different materials are relatively close, they will expand at a similar rate, thus reducing the value of Von stress[13-15].

4. Conclusions

The temperature field of IGBTs and the ageing process caused by the stress of the bonding wire and solder layer are related to a number of factors. The objective of this study is to examine the CTE of heat flux, bonding wire, and solder layer. A finite element analysis was conducted using the COMSOL software to construct a welded IGBT module and establish a thermal-stress coupling field for the purpose of investigating the influence of the aforementioned factors.

(1) The temperature distribution of the IGBT is illustrated on the chip shell, exhibiting a decline from the centre to the edge of the IGBT chip. The temperature of the DBC surface is markedly lower than that of the solder layer. Von Mises stress is primarily concentrated at the root of the bonding wire and the edge of the solder layer. An elevated von Mises stress level increases the probability of a bonding wire fracture and solder layer degradation.

(2) The variation in heat flux has a direct impact on the temperature of the IGBT chip shell, which results in a reduction in the overall temperature of the IGBT chip. A reduction in heat flux is predicted to result in a notable decline in the maximum von Mises stress at the root of the bonding wire and the edge of the solder layer. This is anticipated to provide a means of effectively alleviating the ageing and module failure caused by stress.

(3) The alteration of the coefficient of thermal expansion (CTE) results in fluctuations in the maximum von Mises stress experienced by the bonding wire and the solder layer. It is anticipated that the minimum value will be observed at a specific CTE value. As a consequence of the discrepancy in CTE, the thermal stress is concentrated at the interface of the connecting material, which will ultimately result in the fatigue failure and failure of the bonding line. The experimental data demonstrate that the selection of materials with a similar CTE helps to reduce the risk of stress concentration and thermal

fatigue.

References

[1] Eckert J J ,Társis Prado Barbosa, Silva S F D ,et al.Electric hydraulic hybrid vehicle powertrain design and optimization-based power distribution control to extend driving range and battery life cycle[J]. Energy Conversion and Management, 2022, 252:115094.DOI: 10.1016/j.enconman. 2021. 115094.

[2] Tanriverdi O, Yldrm D. Independent closed loop control of di/dt and dv/dt for high power IGBTs [J].Turkish Journal of Electrical Engineering & Computer Sciences, 2022, 30(3). DOI:10.55730/1300-0632.3793.

[3] Tanrverdi O, Yildirim D. Analog dv/dt and di/dt Controlled Gate Driver With Self-Triggered Hold-at-Zero Algorithm for High-Power IGBTs[J].IEEE Transactions on Power Electronics, 2024(1 Pt.2):39.DOI:10.1109/TPEL.2023.3316260.

[4] Heimler P, Guenther M, Kuenzel J B T .Influence of thermal interface material using discrete Si-IGBTs and consideration of power cycling conditions[J].Microelectronics and reliability, 2023, 150(Nov.):1.1-1.7.

[5] Lahlaci M E, Miloudi M, Miloudi H .Experimental electromagnetic compatibility of conducted electromagnetic interferences from an iGBT and a MOSFET in the power supply[J].Electrical Engineering & Electromechanics, 2024(3).DOI:10.20998/2074-272X.2024.3.05.

[6] Wu Z .A Review of Symmetry-Based Open-Circuit Fault Diagnostic Methods for Power Converters [J].Symmetry (20738994), 2024, 16(2).DOI:10.3390/sym16020204.

[7] Kozak M, Gordon R .A Novel Method for Diagnosing Power Electronics Devices Using Elastic Wave Emission[J].energies, 2023, 16(21).DOI:10.3390/en16217405.

[8] Aretxabaleta I, Inigo M D A, Ignacio Garate J,et al.Multiple current amplifier-based gate driving for parallel operation of discrete SiC MOSFETs[J].IET Power Electronics, 2022(4):15.DOI: 10.1049/ pel2.12232.

[9] Zhang H, Zuo D, Li Y .High-power three-phase interleaved parallel NPC structure DC-DC converter modeling and simulation[J].IOP Publishing Ltd, 2024.DOI:10.1088/1742-6596/2831/1/ 012006.

[10] Li Q, Bian R, Fang X,et al.Fast locating method of MMC lower tube IGBT open-circuit fault based median error between the actual and the predicted value of the capacitor voltage[J].Energy Reports, 2022.DOI:10.1016/j.egyr.2022.02.001.

[11] Das S C, Narayanan G .Thermo-sensitive electrical parameters of high-power IGBTs based on gate-mitter voltage measurement during switching delay intervals[J].Microelectronics and reliability, 2023(Dec.):151.DOI:10.1016/j.microrel.2023.115258.

[12] Wang X, Lu X, Chen W,et al.A half-bridge IGBT drive and protection circuit in dielectric barrier discharge power supply[J].Circuit world, 2022.DOI:10.1108/CW-11-2020-0329.

[13] Prakobsant A , Prastiyanto D , Photong C .Optimum Power-Weight Ratio for Dual 3-Phase Induction Motor Drives for Regenerative Power Maximization[J].Przegląd Elektrotechniczny, 2024(7). DOI:10.15199/48.2024.07.51.

[14] Shahjalal M, Shams T, Hossain S B,et al.Thermal analysis of Si-IGBT based power electronic modules in 50kW traction inverter application[J].e-Prime - Advances in Electrical Engineering, Electronics and Energy, 2023, 3.DOI:10.1016/j.prime.2023.100112.

[15] Schuler L, Chamoin L, Khatir Z,et al.A Reduced Model Based on Proper Generalized Decomposition for the Fast Analysis of IGBT Power Modules Lifetime[J].Journal of electronic packaging: Transactions of the ASME, 2022.