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AI-Enabled Teaching Reform of a Millimeter-Wave Amplifier Design Course: Accelerating Passive Synthesis with RFIC-GPT for a 30 GHz Noise-Cancelling LNA Case Study

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Abstract: *This paper reports a teaching reform for the micro-major course "Millimeter-Wave Amplifier Design" within the "Advanced Chip Design and Innovation" track. Confronting limited contact hours and the cross-disciplinary nature of mmWave IC design, we integrate an RFIC-GPT tool to automate the transformer/inductor synthesis, shortening passive layout iteration and lowering entry barriers. A representative 30 GHz transformer-coupled, noise-canceling LNA serves as the anchor case to link theoretical trade-offs with a design workflow (specification input, schematic design, AI-assisted passive layout generation, EM extraction, final co-simulation). Past semesters of practice show ~25% average reduction in passive design time and sustained student engagement. Results evidence AI-augmented exemplars effectively enhancing IC talent cultivation.*

Keywords: *Millimeter-Wave Education, Low-Noise Amplifier, AI-Assisted EDA, Passive Synthesis, Noise Cancellation, Practical Teaching Reform, Micro-Major Curriculum*

1. Introduction

Integrated circuits underpin modern industry, while advances in scaling, heterogeneous integration, and design automation drive national competitiveness and supply chain resilience [1-2]. 5G and emerging 5G-Advanced use cases intensify demand for phased-array receivers with adaptive beamforming, multi-band aggregation, wide dynamic-range low-noise front ends, and energy-efficient massive MIMO. At millimeter wave (mmWave) frequencies, path loss, blockage, and spectrum fragmentation necessitate tightly integrated low noise amplifiers (LNAs), mixers, synthesizers, phase shifters, and calibration engines in an advanced CMOS platform [3-6]. For China, advancing indigenous mmWave IC capability reduces reliance on imported modules and enables growth in smart manufacturing, vehicular radar, satellite internet, and immersive computing—driving urgent cultivation of cross-disciplinary RFIC talent and artificial intelligence (AI)-enabled design proficiency [7-10].

Recently, micro-majors have gained traction for delivering compact yet rigorous training. Since 2020, our "Advanced Chip Design and Innovation" undergraduate micro-major has coupled distilled theoretical foundations with intensive, workflow-oriented practice. Core courses include Frontier Lectures on Integrated Circuits; Modern Operational Amplifier Technologies and Applications; Principles and Design of Low Phase-Noise VCOs; Principles and Design of Low-Power PLLs; Asynchronous Timing SAR ADC Technologies and Design; and mmWave Amplifier Design. The last one, taught by the first author of the article, aims to build a deep understanding of mmWave amplifier theory, low-noise design strategies, and representative power-combining approaches. Its scope spans device-level principles, topology selection, design flow partitioning, simulation and verification of low-noise and power amplifiers, layout/routing heuristics, and current trend awareness in high-frequency mmwave front ends.

Persistent challenges remain: limited contact hours (32), a broad, vertically integrated knowledge stack, and high iteration overhead in passive and electromagnetism (EM)-aware design. The question is how to extract high-leverage concepts, translate them into authentic design capability, and remains on schedule. Recent advances in AI present leverage points. Departing from conventional manual passive synthesis, we integrated an AI tool of RFIC-GPT into the LNA practical module. Students provide a

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small set of electrical targets; the web service returns multiple synthesized passive layout candidates with extracted parameter summaries. Learners select a candidate, import it into the EDA environment, co-simulate with the active transistor core, and iterate toward specification closure. This reduces trial-and-error friction in geometry drafting and accelerates convergence; over two semesters, students achieved ~25% reduction in design iteration time while meeting preset performance goals. To align with talent-cultivation goals, we anchored the practical sequence around a representative transformer-coupled noise-canceling (NC) LNA previously investigated in our laboratory [11–14]. This research-grade exemplar offers pedagogical value: passive–active co-design sensitivities and measurable EM vs schematic divergence. Embedding such an authentic circuit fosters disciplined troubleshooting, strengthens innovation orientation, and sustains intrinsic motivation to explore beyond template solutions.

2. Background on mmWave LNA design

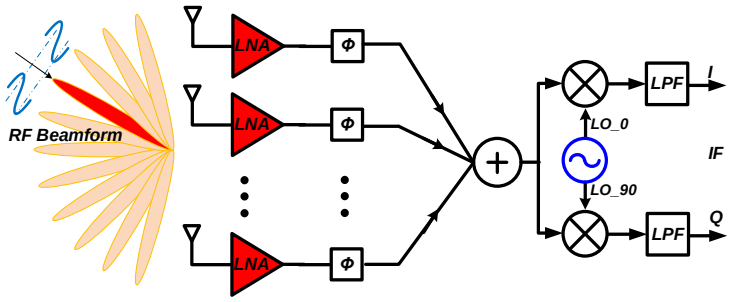

Figure 1: General diagram of phase array receiver.

A primary objective of an mmWave N-element phased-array receiver (Rx) in Figure 1 is to acquire high-throughput data while performing agile beamforming that selectively enhances desired signals and suppresses or spatially filters unwanted interferers. Typical front-end building blocks include LNAs, phase shifters, local oscillators or frequency synthesizers, mixers, power combiners, channel-select or anti-alias filters, and patch antennas [15-21]. Among these, the LNA critically constrains the minimum achievable system noise figure (NF); as array sizes scale, lnas must simultaneously push toward lower power consumption, lower NF, higher operating frequency, and wider bandwidth.

Fundamental mmwave LNA design requires coordinated optimization of active and passive devices under specification constraints. Passive structures such as transmission lines and transformers dominate insertion loss, bandwidth, and impedance transformation quality, thereby exerting a decisive influence on overall noise and gain performance. Active device choices and bias conditions set transconductance, noise contributions, linearity headroom, and robustness to PVT variations.

Widely applied to numerous small-signal amplifying scenarios, the LNA is a fundamental device to amplify wanted signals while introducing undesirable noise as marginally as possible. Its main specifications cover frequency range, gain, noise figure, linearity, and power consumption[22-27]. The frequency range is meant for the spectrum of frequencies that the LNA can fully cover. The gain indicates the ability of small signal amplification, while the NF means the deterioration level of the signal-to-noise ratio. Linearity reflects the capability of the LNA to handle unwanted in-band interference. Power consumption represents the electrical energy consumed by the circuit during operation. Balancing these metrics entails trade-offs (e.g., higher bias current improves NF and linearity but increases power; aggressive matching may reduce NF while narrowing bandwidth). Modern design flows therefore integrate EM-accurate passive modeling, device noise parameter extraction, and iterative co-optimization to converge within layout-aware constraints.

3. Experimental workflow and implementation

Experimental Objective: This experiment guides the design of a mmWave LNA using a transformer-coupled topology in a 65 nm CMOS process. Students will become proficient with EMX, Cadence, and the AI tool RFIC-GPT. They are expected to complete the standard flow: specification definition, schematic design, layout, and circuit–EM co-simulation. A key objective is to experience the efficiency gains provided by the RFIC-GPT in passive structure synthesis.

Experimental Requirements: Students must understand each technical specification of a mmwave LNA and master the corresponding design methods. Target specifications: center frequency ≈30 GHz;

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bandwidth >6 GHz; ~ 20 dB gain; NF <4 dB; input referred IP3 > −10 dBm; and minimal DC power.

In designing the mmWave LNA, first things first are to determine the design specifications, followed by the schematic design where the passive components, such as transformers and inductors, just use library parts besides the active devices incorporating parasitics. In this design phase, students are guided to pay more attention to the general technical points, including NC and bandwidth coverage. The former are mapped to the active design, as discussed in Part 3.2. The bandwidth coverage, however, has a close relationship with the resonant tank, or equivalently, the transformer design and optimization in terms of inductor value and coupling factor. In the layout design phase, active layout work can be partially accelerated by the Virtuoso design tool of parametric transistors. In contrast, the passive layout design is heavily dependent on EM simulation, traditionally. Typically, a designer should convert the parameters of a transformer to a physical implementation. First, draw a tentative mental routing in a software environment, say ADS, and then do EM simulation, and finally compute the extracted parameter of the layout and compare it to the initial parameter input. Depending on the designer's experience, this process is usually time-consuming and requires lots of iterations, as shown in Figure 2, between layout adjustment and EM simulation to meet the desirable goals. Subsequently, the overall circuit is simulated by extracting all passive components and routing connections in both passive and active layout partitions. According to the simulation results, a slight adjustment of parameters may be needed and applicable for the layout of the passive partition. Since the mmWave designs are comparatively sensitive to parasitics and routing loss, a local optimization of the passive layout is necessary. Once the performance of the overall circuit meets the design specifications, the iterative adjustment terminates. The specific process as described above can be vividly illustrated in Figure 2.

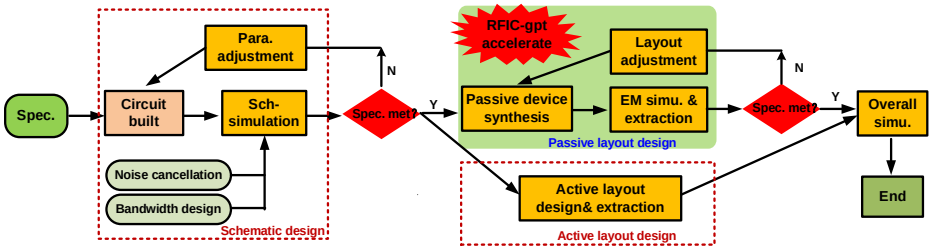

Figure 2: Design workflow of mmWave LNAs.

3.1 RFIC-GPT-driven Passive Transformer Synthesis

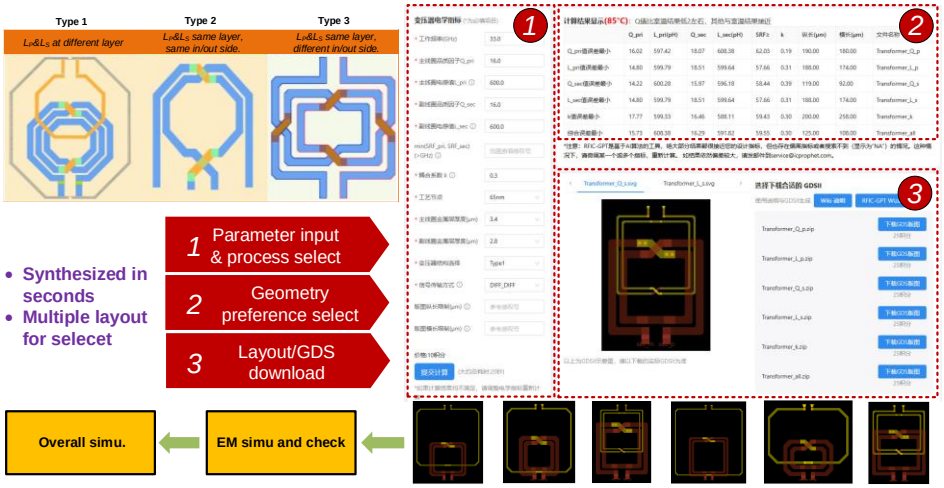

Figure 3: Workflow of transformer synthesis assisted by RFIC-GPT.

Recently, AI has been changing our traditional development pattern of technical work significantly. For example, the appearance of RFIC-GPT is effective in handling those tedious iterative computations and frees designers from doing the boring work in at least two aspects. Firstly, mmWave IC design requires interdisciplinary foundations in microwave engineering, electromagnetics, and circuit theory. During design, one must understand how each parameter influences overall performance; the sheer number of parameters and the complexity of their interactions often discourage beginners. The RFIC-GPT Online helps students quickly learn how a given parameter impacts the outcome, sparing mentors from repetitive instruction and allowing students to accumulate rich experience through iterative

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experimentation. Secondly, although students should still possess the ability to draft the required layouts themselves, the highly repetitive and tedious follow-up work often leads to frustration—especially in complex IC design. Obtaining a usable layout in an extremely short time reduces the time cost and helps sustain learning motivation. Luckily, the computational results provided by the RFIC-GPT can be used directly, and in special cases, minor layout adjustments can further satisfy specific needs.

Transformers and inductors are two widely utilized components for mmWave ICs [28-30]. Especially, the transformer has shown a more flexible design advantage by tuning the additional coupling factor k while maintaining an equivalent footprint to an inductor. On-chip transformers exploit the mutual inductance of adjacent conductors to transfer electromagnetic energy from one coil to another, achieving signal transmission. As a thumb rule, it is wise to route transformer's traces into thick metal layers, often adopting an octagonal structure for a better quality factor.

With the aid of the deft RFIC-GPT tool, one can easily observe any design tradeoff of passive components, say, the inherent compromise of inductors between inductance value and quality factor. More beneficially, a passive component can be synthesized instantly in seconds. Typically, a series of target electrical specifications (e.g., transformer: quality factor Q/ inductance L/ coupling factor k) provided from the schematic simulation can be input at the online interface of the tool, as in the top right corner of Figure 3 where the specific process, trace routing layer, signal input/output style, and coil coupling structure are also determined by designers. The tool renders three types of coil coupling structures, as shown in the upper-left corner of Figure 3, for users to select. After collecting all these information constraints, it then leverages AI algorithms to generate—within seconds—a couple of synthesized devices and circuit GDSII layouts that meet the requirements, with different metric emphasis and resulting geometry characters as manifested at the bottom right of Figure 3. Depending on the designer's preference, any of the generated results can be directly exported to a top-level circuit simulation.

3.2 Noise-Cancelling Active Path Design

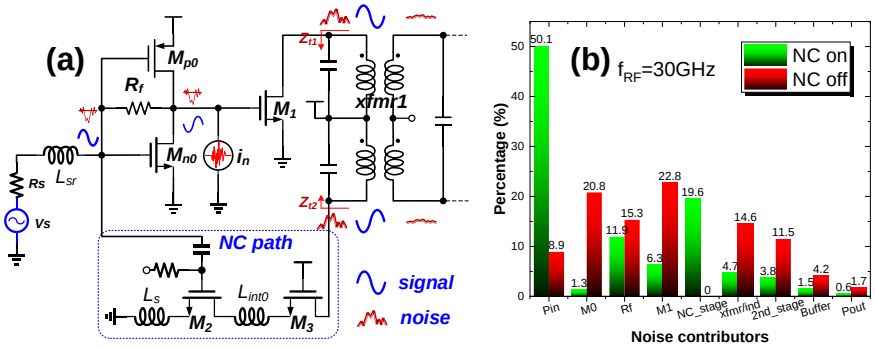

Figure 4: (a) Noise cancellation LNA illustration. (b)Noise percentage contribution.

Show in Figure 4(a) is the noise flow of M_0. It flows forward to the Z_{t1} load of one parallel LC tank while going through the NC path to the Z_{t2} load of another LC tank. The two noises are in phase in principle, and the resulting noise-cancelling condition [11,22] is shown as

$$1+\frac{R_f}{R_s}=\frac{g_{m2}}{g_{m1}}\cdot\frac{Z_{t2}}{Z_{t1}} \tag{1}$$

Where the parameter g_{mx} (x takes 1~2) represents the small-signal transconductance of M_x transistor, while R_f and Rs are the feedback and source resistors. The Z_{t1} and Z_{t2} are the impedance of two LC tanks consisting of capacitors and the primary coil of $xfmr_1$. Furthermore, the signal flow also goes through the main and NC paths, respectively. But the resulting two amplified signals at the Z_{t1} and Z_{t2} are out of phase, and the difference between them is in superposition and transferred to the next stage. Here, the $xfmr_1$ is designed in symmetry, and the ratio of g_{m2}/g_{m1} is used to balance the NC amplitude requirement. Practically, the M_2 can use much larger transconductance to suppress its noise output sufficiently, instead of exactly following the NC condition. Thus, the amplitude requirement in (1) is relatively resilient. Furthermore, under the mmWave frequencies, the phase inevitably changes due to parasitics of transistors, potentially undermining the phase requirement embedded in (1). By slightly shifting the resonating frequency point of Z_{t2} to a higher frequency, the resulting lead phase offset compensates for the phase error lag by the NC path, roughly meeting the NC phase constraint. Favorably, based on a

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symmetric transformer structure, the presented NC via adjusting the proper ratio of g_{m2}/g_{m1} and the tank's resonating point is more efficient than traditionally conducting time-consuming EM simulations to seek the optimized windings' ratio of asymmetric transformer footprint which also cannot be accelerated by the RFIC-GPT tool. Figure. 4(b) displays noise percentage contributions by individual parts, obtained from Spectre simulations with transformers/inductors extracted. When the NC path is disabled, except for the input port, several dominant noise sources are M_0, M_1, and R_f. In comparison, once the NC path is switched on, the noise contributions by the M_0, M_1, transformers, and even the second stage are sufficiently suppressed, although the noise by M_0 still exists, and the NC path, in turn, yields an appreciable noise component.

3.3 Two-Stage LNA Architecture and Representative Results

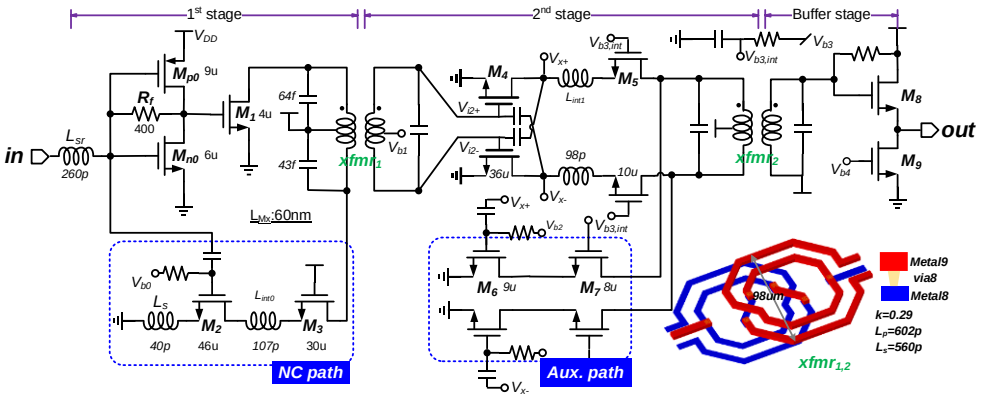

Figure 5: Complete schematic of two-stage LNA.

Since a single stage usually provides limited gain, an additional stage is thus cascaded and makes the final circuit a two-stage structure, while the output buffer stage is only for the test target and gets removed in practical phased array applications. To facilitate the students' learning and comparison, both simulation and measurement are displayed below for reference, although only simulation results are required by the course. The mmWave LNA circuit was fabricated in a 65 nm CMOS technology. The bare chip was measured via on-chip probes. The buffer effect is de-embedded from the measured results below. and the micrograph is displayed in Figure.7(b), occupying an active area of 869×274 um^2. Under a 1.2 V supply voltage, the power of the LNA core excluding the output buffer is 17.8 mW. The values of devices are shown in Figure 5, where the transistors' length takes a minimal 60 nm. Accordingly, students can quickly complete the schematic design and obtain the desired electrical metrics. Meanwhile, the passive components of inductors and transformers are simulated with electrical parameters of L/Q/k, which are then imported into the RFIC-GPT interface to instantly synthesize the wanted passive layout with the least iterations, as mentioned in Figure 3. The active layout can be designed in a centroid floorplan or a round table style. Finally, students are to merge the two layouts and do the whole simulation based on the extracted layout data. Their simulations should approach the proficient design results displayed below. Considering their insufficient experience during the learning period, the specifications defined above are fairly loose.

Here, some common configuration guides are explained for the EDA software, taking Cadence as an example. Specifically, when doing S-parameter simulation to obtain S11, S22, and gain, an SP Simulator is solely used where students need to set a larger frequency scanning range, say 20-45 GHz, and leave the step size as default, and choose the linear scale of the horizontal axis. By clicking the 'run' button, one can get the desired curves by further ticking the output metric option at the 'direct plot' menu. Again, at the SP simulator panel, clicking the noise option enables the NF computation output function. For the linearity simulation, a PSS simulator is selected, where a fundamental tone as a large signal is fixed at 30 GHz, and a harmonic number of 10 is recommended. Further enabling the PAC simulator, setting a point frequency of 30.01 GHz and the harm number: 3, complete all the panel setup. In the schematic view, edit the property of the input port and fill in the input signal power, say -30 dBm, as the power of the fundamental tone and PAC tone. One can then simulate to get the plot of linearity.

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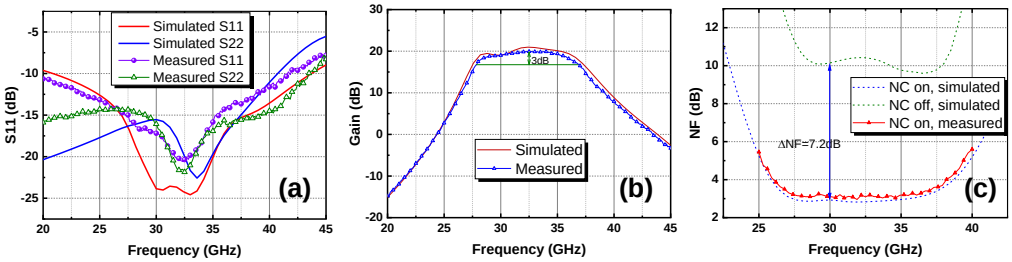

Figure 6: Performance results of (a) S11/S22,(b) gain, and (c)NF results.

As illustrated in Figure 6(a), the input and output reflection characteristics meet wideband matching targets, with S11 maintained below -10 dB across 20–42 GHz, and S22 exhibiting an even broader interval below the -10 dB threshold, thereby reinforcing the instructional objective of imparting practical insight into broadband impedance design. The comparative simulation–measurement study of forward gain in Figure 6(b) shows a measured peak S21 of approximately 20 dB and a -3 dB gain bandwidth spanning roughly 28–37 GHz, aligning with the preset design specifications and offering students a concrete case of gain–bandwidth trade-off evaluation. Noise performance, presented in Figure 6(c), demonstrates an average in-band noise figure (NF) of 3.1 dB, while controlled simulation experiments further reveal a 7.2 dB NF degradation when the noise-cancellation (NC) path is intentionally disabled. This differential outcome is used pedagogically to guide learners in isolating architectural contributions to system-level noise optimization. Although not explicitly plotted, comprehensive stability simulations confirm unconditional stability across the operating spectrum, which is emphasized in class to reinforce rigorous verification habits rather than reliance on isolated performance metrics. Overall, this dataset serves as an integrated teaching module linking theoretical scattering parameter analysis, architectural noise suppression mechanisms, and systematic validation workflows.

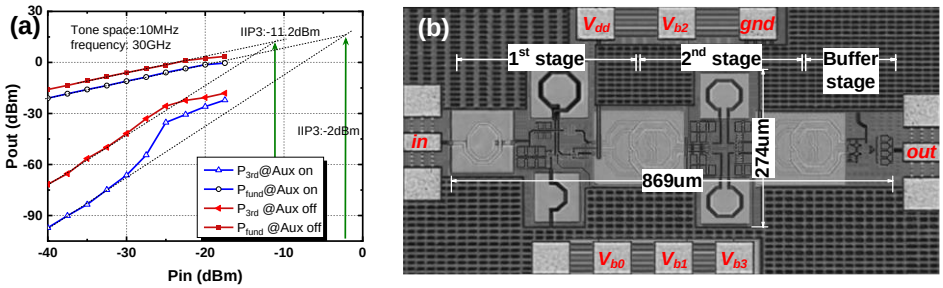

Figure 7: (a) Linearity of IP3. (b) Chip micrograph.

As depicted in Figure 7(a), a standard two-tone intermodulation method [31-36] is employed to contextualize linearity evaluation for students. Under controlled bias conditions, disabling the auxiliary path (V_{b2} = 0 V) yields a measured IIP3 of -11.2 dBm at the 30 GHz center frequency, whereas enabling the path (V_{b2} = 0.49 V) elevates the IIP3 to -2 dBm. The improvement is ascribed to the derivative superposition technique [27-28]. This contrast is intentionally used in instruction to help learners internalize how auxiliary circuit branches contribute to third-order distortion suppression. Following activation of the auxiliary path, the measured input 1 dB compression point IP1dB is -18.2 dBm, offering a concrete reference for correlating large-signal compression with small-signal intercept metrics[37-43]. Pedagogically, this dataset serves to: (1) exemplify rigorous linearity characterization methodology; (2) cultivate students' ability to interpret the correlation of IIP3 and IP1dB; and (3) encourage evidence-based reasoning when justifying architectural enhancements.

To substantiate the ~25% reduction in passive layout plus EM tuning time, we compared a 2024 baseline cohort (32 enrolled; complete time-log sample n=18) with a 2025 reform cohort integrating RFIC-GPT (35 enrolled; sample n=20) under the identical 30 ghz transformer-coupled LNA specification. In 2024, students manually iterated transformer and inductor geometries, averaging 6.7 EM extraction loops (σ=1.9) before convergence; the mean passive synthesis and verification effort (from auditable design log timestamps and weekly time sheets) was 11.2 hours per team. In 2025, average EM loops fell to 4.9 (σ=1.4) and effort to 8.4 hours, yielding a 25.0% mean time differential ((11.2−8.4)/11.2). Debriefs attribute savings to (1) instant multi-candidate generation spanning diverse k–L–Q trade spaces, (2) elimination of initial geometry drafting, and (3) faster triage of suboptimal topologies via structured parameter summaries. No degradation in final spec attainment or report rubric scores was observed despite variance for weaker CAD backgrounds.

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4. Conclusion and Outlook

This reform of the "Millimeter-Wave Amplifier Design" micro-major course shows that targeted AI assistance can measurably compress iteration while deepening conceptual linkage between architecture and metrics. Embedding RFIC-GPT for transformer/inductor synthesis reduced passive layout plus EM tuning time by about 25%, enabling more space for analysis of gain–noise–linearity trade-offs and verification discipline. The 30 GHz transformer-coupled noise-canceling LNA case provided tangible anchors: wideband input/output match (S11 < -10 dB over 20-42 GHz), ~20 dB peak gain with 28-37 GHz -3 dB window, 3.1 dB noise figure versus a 7.2 dB penalty when NC is disabled. These quantified contrasts strengthened students' evidence-based reasoning and troubleshooting confidence. Remaining gaps include expansion of AI support beyond passive synthesis, finer assessment of higher-order design thinking, and validation across larger cohorts and additional RF blocks. Future work targets multi-objective co-optimization, adaptive feedback, and automated robustness analytics.

Acknowledgment

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